LINEAR TECHNOLOGY

NOVEMBER 1998 VOLUME VIII NUMBER 4

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World's Smallest 24-Bit ADC Packs High Accuracy, Ease of Use, into SO-8

by Michael K. Mayes

Introduction

Linear Technology enters the delta-sigma[1, 2] analog-to-digital converter market with a tiny, high performance, 24-bit ADC, the LTC2400. The device's superiority to existing delta-sigma ADC's results from the combination of an accurate analog modulator with an innovative new digital architecture. Typically, fine-line, digitally optimized processes are required for a delta-sigma ADC's on-chip digital filter. The resulting ICs have high pin counts, large packages and complex interfaces. The LTC2400's breakthrough in digital filtering allows the use of an analog-optimized process. The result is the smallest (SO-8 package), lowest pin count (8) simplest to use delta-sigma converter on the market. A highly accurate on-chip oscillator, using Linear's high performance CMOS process, sets the digital filter's notch frequency, eliminating the need for an external crystal. Additionally, the part offers exceptional INL, DNL, noise and 50Hz/60Hz rejection. The innovation does not end here; this article will show how performance, ease of use and functionality make this part the new state of the art in high resolution delta-sigma ADCs.

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Overview

The analog modulator is critical to the performance of a delta-sigma ADC. For high DC accuracy, 1st or 2nd order modulators provide insufficient differential nonlinearity (DNL). The LTC2400 achieves optimum DC performance from a 3rd order delta-sigma modulator (see Figure 1). Feedforward compensation and analog processing within the modulator eliminate instability issues associated with high order modulators. The 1-bit ADC and DAC within the modulator guarantee monotonicity and exceptional INL performance of 4ppm.

The output of the delta-sigma modulator is applied to a decimating filter. The sinc[4] filter removes the quantization noise from the modulator output. Additionally, this filter rejects the fundamental frequency and its harmonics. This notch frequency is set by an on-chip oscillator, typically at line frequency for DC applications. The combination of a 4th order sinc filter with a precision thin-film, factory-trimmed oscillator guarantees at least 120dB rejection of line frequency ±2%. Several converters on the market use sinc[3] or sinc[1] filters. Since line frequencies can vary up to 2% over a 24-hour period, converters using these lower order filters cannot achieve 120dB

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Issue Highlights

Our cover article for this issue introduces Linear Technology's entry into the delta-sigma analog-to-digital converter market: the tiny, high performance, 24-bit LTC2400. The LTC2400's superiority to existing delta-sigma ADC's results from the combination of an accurate analog modulator with an innovative new digital architecture. The LTC2400's breakthrough in digital filtering allows the use of an analog-optimized process. The result is the smallest (SO-8 package), lowest pin count (8) simplest to use delta-sigma converter on the market.

Our Design Features section debuts three new power products. The LT1676 and LT1776 are Linear Technology's latest offerings for high voltage (to 60V) step-down switching regulator applications. The LT1676/LT1776 operate in a fixed frequency mode (100kHz for the LT1676 vs 200kHz for the LT1776) and can be externally synchronized to a higher switching frequency. The internal output switch is rated at a nominal peak current of 700mA, which typically accommodates DC output currents of up to 500mA.

The LTC1622 step-down DC/DC controller is designed to harness all the energy from lithium-ion batteries. Its wide input-voltage range and 100% duty cycle allow low dropout for maximum energy extraction from the battery. Its low quiescent current extends battery life. High frequency operation allows the use of small inductors, making it ideal for communications products.

In addition, this issue introduces two new comparators. The LT1720 is an UltraFast™, low power, single-supply, dual comparator designed to operate on a single 3V or 5V supply. The comparators feature internal hysteresis, making them easy to use, even with slowly moving input signals. The LT1720 is fabricated in Linear Technology's 6GHz complementary bipolar process, resulting in unprecedented speed for its low power consumption.

The LTC1531 is an isolated, self-powered comparator that receives power and communicates through internal isolation capacitors. The isolation capacitors provide $3000V_{RMS}$ of isolation between the comparator and its output. This allows the part to be used in applications that require high voltage isolated sensing without the need for an isolated power source.

In the amplifier arena, we premier the LT1468, a single op amp optimized for accuracy and speed in 16-bit systems. Operating from ±15V supplies, the LT1468 in a gain of –1 configuration will settle in 900ns to 150µV for a 10V step. It also features the excellent DC specifications required for 16-bit designs. Two key applications are current-to-voltage (I/V) conversion following a fast, 16-bit current output digital-to-analog converter (DAC) and buffering the input of an analog-to-digital converter (ADC).

One of the first products from LTC's new proprietary high speed bipolar process is a 250MHz RGB (red, green, blue) multiplexer that is optimized for switching speed. This new MUX, the LT1675, is designed for pixel switching in video graphics and for RGB routing. It is configured with three SPDT RGB video switches and three current feedback amplifiers for direct driving of cables.

Our two Design Ideas for this issue are a PolyPhase supply based on two LTC1430As operating 180° out of phase, and a current feedback video amplifier with a level shifter for ground-referenced signals.

Our Design Information section features the conclusion of Jim Williams's exposition on measuring 16-bit DAC settling time, and also introduces the LTC1545, a Net1 and Net2 compliant serial interface chip that supports the optional Test Mode, Remote Loopback and Local Loopback functions.

We conclude with a septet of New Device Cameos.

LTC in the News...

Linear Technology Corporation announced its first quarter financial results on October 13, 1998, reporting net sales of $116,032,000—an increase of 6% compared to the same period last year. The Company's net income for the quarter, $44,382,000 or $0.56 diluted earnings per share, was up 9% compared to the first quarter of last year. Linear Technology also reported that during the quarter it purchased back 1,800,000 shares of its common stock at a cost of approximately $100,000,000. In discussing the results, President and CEO Robert H. Swanson noted that the Company continued to have outstanding profitability and Linear Technology's return on sales for the quarter "was both a record for the Company and the strongest in the industry."

Linear Technology's new delta-sigma analog-to-digital converter, the LTC2400 (see page 1), was the cover story of the September issue of *Electronic Design*. The article detailed the LTC2400's exceptional speed, precision and ease-of-use, and included a range of illustrations highlighting the LTC2400's 24-bit differential nonlinearity with no missing codes. The article also underscored this new part's groundbreaking design, allowing it to be housed in a tiny SO-8 package yet deliver superior performance compared to competing parts more than twice its size.

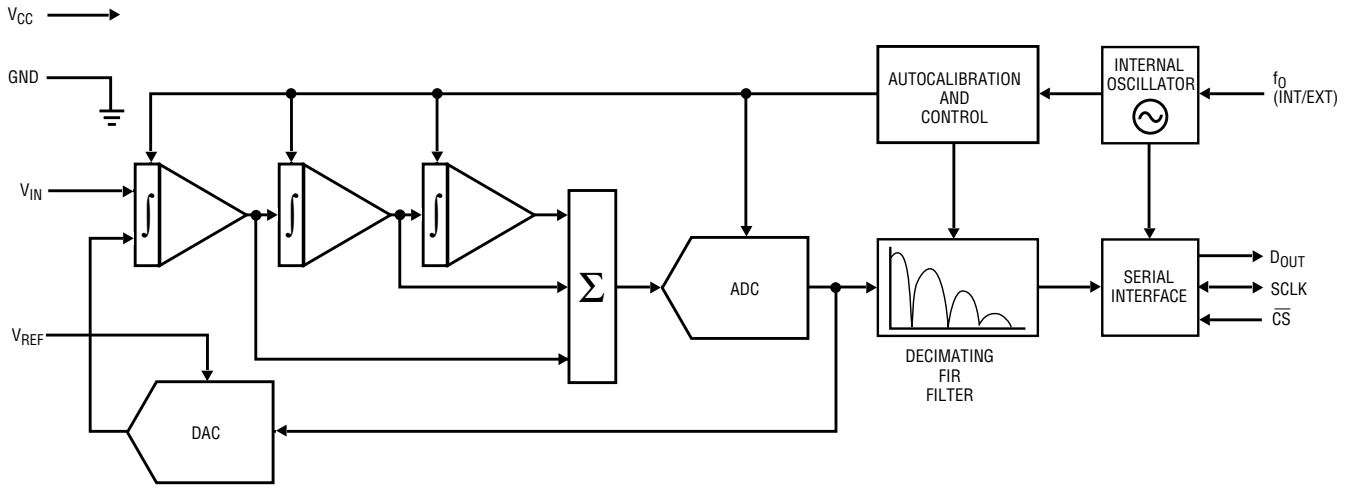

Figure 1. LTC2400 block diagram

LTC2400, continued from page 1

rejection, even with exact external oscillators (refer to Figure 6a).

A simple, SPI-compatible 3-wire interface outputs data with single-cycle settling. This simplifies the user interface by eliminating latency and redundant data normally associated with delta-sigma ADCs. As a black box, the converter resembles traditional, easy-to-use converters.

Performance

Designed on a 2µ, single-metal, analog CMOS process, the LTC2400 is implemented with a die size under 10kmil^2. The key to Linear attaining the nearly impossible is the highly efficient sinc^4 filter. Once the tiny digital circuitry was completed, the analog circuitry was optimized for ultrahigh performance.

The result is 24-bit DNL with no missing codes guaranteed. As shown in Figure 2, the integral nonlinearity is a mere ±2ppm or 0.0002%. This compares favorably with other 24-bit devices' INL performance of 15ppm–30ppm. Transparent to the user, the converter continuously executes self-calibration algorithms automatically adjusting the offset and full-scale. With an initial accuracy of 1ppm, the offset drifts less than 0.01ppm/°C and the full scale drifts less than 0.02ppm/°C (see Figures 3 and 4). Combining these DC parameters with RMS noise performance of 0.3ppm (see Figure 5), the LTC2400 resembles a 6-digit digital voltmeter on a chip.

The modulator consists of operational amplifiers and switched capacitor circuits. Previous delta-sigma converters place limitations on these circuits. Since the LTC2400 was designed on an analog process, these limitations are removed. This allows a power supply range of 2.7V to 5.5V and a reference range of from below 10mV to 90% of V_{CC}. At V_{CC} = 3V, the power consumption is 750µW; it falls to 45µW in power-down mode.

In many applications, the input signal may exceed V_{REF} or fall below ground. Conventional delta-sigma converters are unable to provide the user with any indication of these overrange conditions. The LTC2400 has on-chip overrange circuitry. It continues to output 24-bit valid data over an effective input range of $-12.5\% \times V_{REF}$ to $112.5\% \times V_{REF}$.

One of the main advantages of delta-sigma converters over SAR or flash-type architectures is the inherent rejection of line frequency. In order to achieve good rejection, past delta-sigma converters required an accurate external oscillator or crystal with a precise, uncommon value. The LTC2400 incorporates an on-chip oscillator eliminating the need for

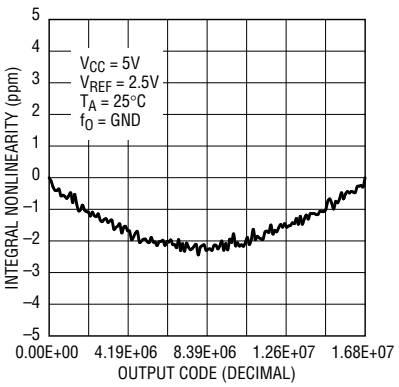

Figure 2. LTC2400 integral nonlinearity error

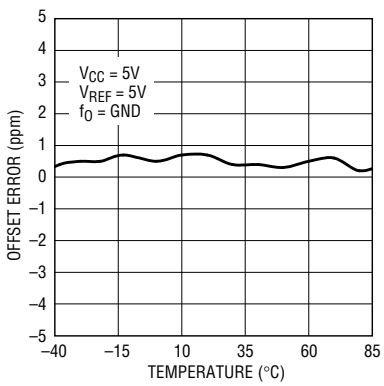

Figure 3. Offset drift

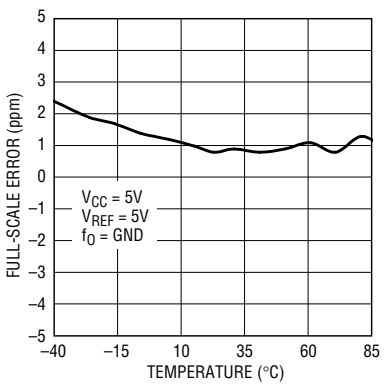

Figure 4. Full-scale drift

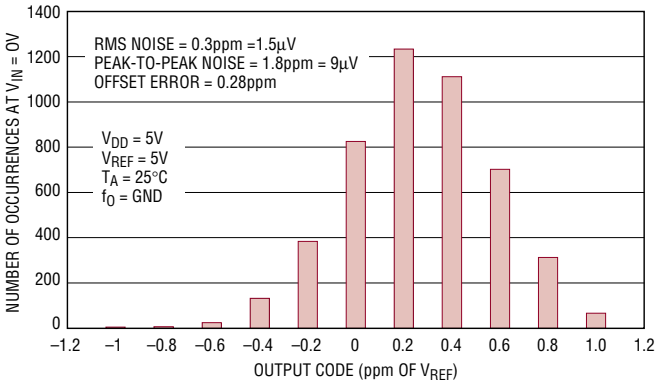

Figure 5. Noise histogram

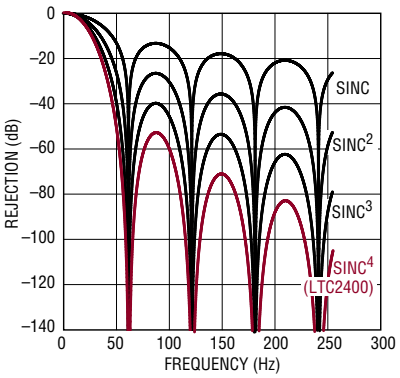

Figure 6a. Filter response vs filter order

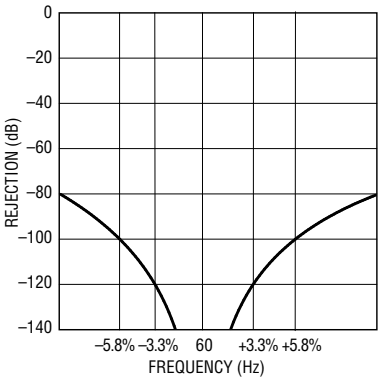

Figure 6b. Filter response at line frequency

external components. The internal oscillator is so precise that the ADC rejects line frequency over a ±2% range, independent of supply or operating temperature (see Figure 6a, where sinc[1], sinc[2] and sinc[3] filters are shown for comparison). Line frequencies of 50Hz or 60Hz are selectable by simply tying the f_O pin to V_{CC} or ground. Other rejection frequencies can be obtained by driving the f_O pin with an external clock.

The converter is so robust that the noise performance and line rejection are insensitive to layout. As shown in Figure 7, large noise errors applied to V_{CC}, V_{REF} or V_{IN} (1.25V_{P-P}, 60Hz, ±2%) have no effect on the ADC's noise and linearity performance.

Ease of Use

At a glance, the LTC2400 looks more like an op amp than a delta-sigma converter. With only eight pins, it's about as easy to use as a common op amp (see Figure 8). Superior noise rejection and internal analog circuitry enable the use of one supply pin, one ground pin and a single-ended input. The internal oscillator eliminates external crystals/capacitors and added device pins. The remaining pins form a standard 3-wire interface, consisting of a three-statable serial data output (D_{OUT}) under the control of a chip select pin ($\overline{CS}$) and a serial data output clock (SCLK).

Applications currently using traditional ADCs can easily migrate to the LTC2400. Single-cycle settling yields a one-to-one correspondence between the start of a conversion and the output word. This allows the user to place a multiplexer in front of the ADC without worrying about latency or data statistically dependent on previous conversion results.

Functionality

Despite its small size and low pin count, the LTC2400 provides many flexible modes of operation. For example, tying $\overline{CS}$ low forces a continuous conversion mode. With $\overline{CS}$ tied high, the device enters a 45µW power-down mode. For applications requiring ultralow power, a capacitor can be tied to $\overline{CS}$. Under this

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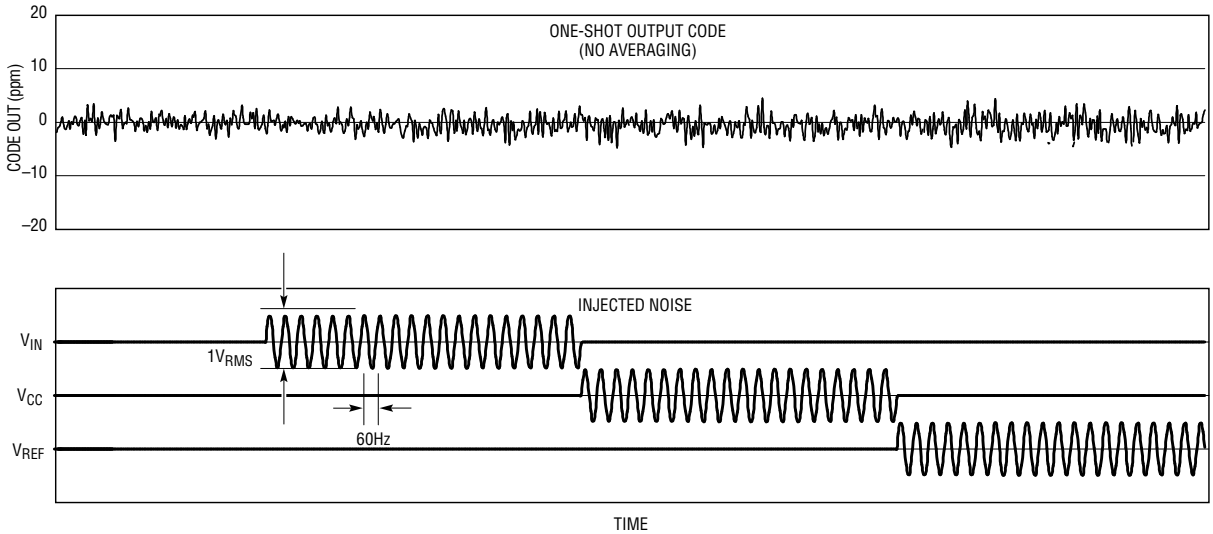


Figure 7. Noise injection

Wide Input Range, High Efficiency Step-Down Switching Regulators

by Jeff Schenkel

Introduction

The LT1676 and LT1776 are Linear Technology's latest offerings for high efficiency step-down switching regulator applications. These two parts are pin-for-pin compatible and virtually identical in operation, the only difference being their internal oscillator frequencies—100kHz for the LT1676 vs 200kHz for the LT1776. They operate in a fixed frequency mode (as opposed to constant off-time or on-time, for instance) and can be externally synchronized to a higher switching frequency.

The internal output switch is rated at a nominal peak current of 700mA, which typically accommodates DC output currents of up to 500mA. The input voltage range is 7.4V to 60V. Maintaining acceptable efficiency in the upper half of this input voltage range requires very fast output-switch edge rates. The LT1676/LT1776 contain specialized output circuitry to deliver this performance. Additionally, they contain circuitry to monitor output load level and reduce leading-edge switch rate (turn-on) when the output load is light. This arrangement helps avoid pulse skipping at light load, with its consequent subharmonic behavior.

True current mode operation is supported, with all its well known advantages for switching regulator operation. The shutdown pin implements a pair of functions. Pulling it down to near ground turns off the part almost completely and reduces the quiescent current to a few tens of microamperes. The second shutdown pin function acts at a threshold of roughly 1.25V. Below this level, the part operates normally, except that output switching action is inhibited. This allows the implementation of an undervoltage lockout function set by, for instance, an external resistor divider. The LT1676/LT1776 are available in both 8-pin SO and PDIP packages.

Theory of Operation

The LT1676/LT1776 are current mode switching regulator ICs optimized for high efficiency operation in high input voltage, low output voltage buck topologies. The block diagram in Figure 1 shows an overall view of the system. Several of the blocks are straightforward and similar to those found in traditional designs, including the internal bias regulator, oscillator and feedback amplifier. The novel portion includes an elaborate output switch section and a logic section to provide the control signals required by the switch section.

The LT1676/LT1776 operate much the same as traditional current mode switchers, the major difference being their specialized output switch section. Due to space constraints, this discussion will not reiterate the basics of current mode switcher/controllers and the step-down topology. A good source of information on these topics is Linear Technology Application Note 19.

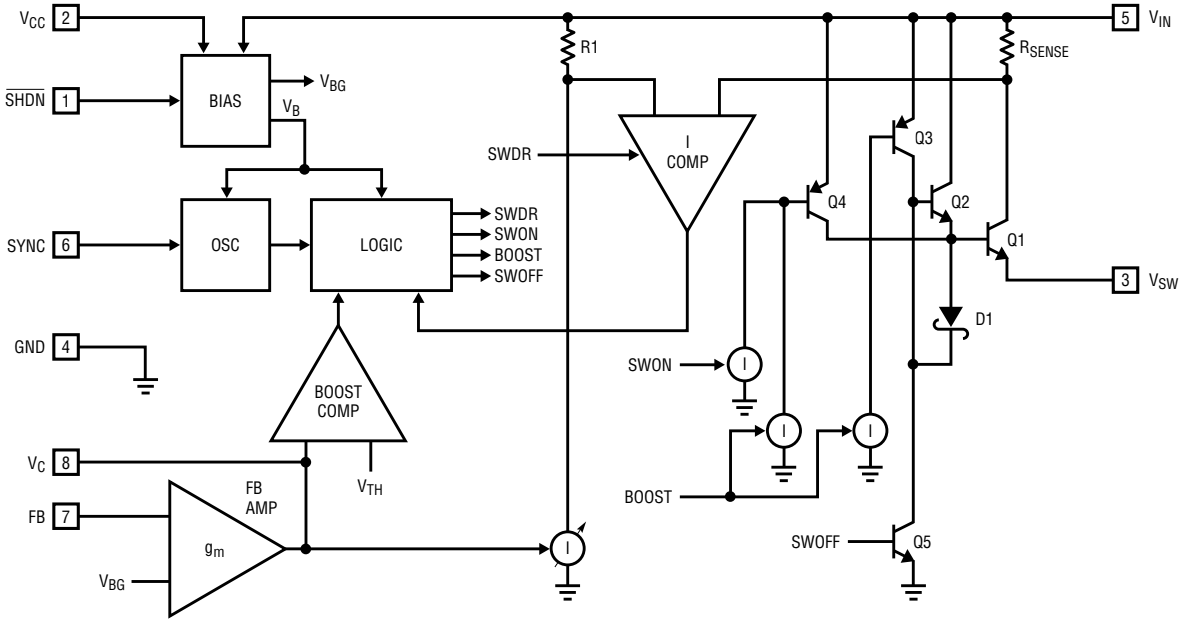


Figure 1. LT1776 block diagram

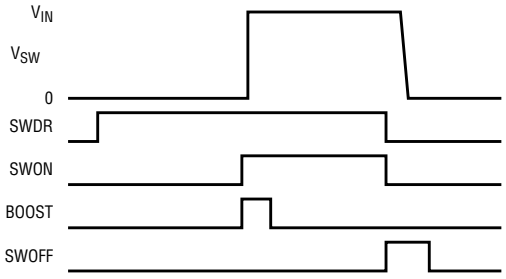


Figure 2a. Timing diagram: high dV/dt mode

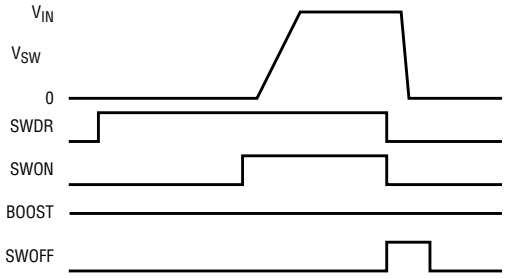


Figure 2b. Timing diagram: low dV/dt mode

One of the classic problems in delivering low output voltage from a high input voltage at good efficiency is that minimizing AC switching losses requires very fast voltage (dV/dt) and current (dI/dt) transitions at the output device. This is in spite of the fact that in a cost-effective bipolar IC process implementation, slow lateral PNPs must be included in the switching signal path.

Fast, positive-going slew rate action is provided by lateral PNP Q3 driving the Darlington arrangement of Q1 and Q2. The extra β available from Q2 greatly reduces the drive requirements of Q3. Although desirable for dynamic reasons, this topology alone will yield a large DC forward voltage drop. A second lateral PNP, Q4, acts directly on the base of Q1 to reduce the voltage drop after the slewing phase has taken place. To achieve the desired high slew rate, PNPs Q3 and Q4 are "force-fed" packets of charge via the current sources controlled by the BOOST signal.

Please refer to the timing diagram of Figure 2a. A typical oscillator cycle is as follows: The logic section first generates a SWDR signal, which powers up the current comparator and allows it time to settle. About 1µs later, the SWON signal is asserted and the BOOST signal is pulsed for a few hundred nanoseconds. After a short delay, the V_{SW} pin slews rapidly to V_{IN}. Later, after the peak switch current, indicated by the control voltage V_C, has been reached (current mode control), the SWON and SWDR signals are turned off and SWOFF is pulsed for a few hundred nanoseconds. The use of an explicit turn-off device (Q5) improves turn-off response time and thus aids both controllability and efficiency.

The system described previously handles heavy loads (continuous mode) at good efficiency, but is actually counterproductive for light loads. The method of jamming charge into the PNP bases makes it difficult to turn them off rapidly and achieve the very short switch ON times required by light loads in discontinuous mode. Furthermore, the high leading edge dV/dt rate has a similar adverse effect on light load controllability.

The solution is to employ a "boost comparator" whose inputs are the V_C control voltage and a fixed internal threshold reference, V_{TH}. (Remember that in a current mode switching topology, the V_C voltage determines the peak switch current.) When the V_C signal is above V_{TH}, the previously described "high dV/dt" action is performed. When the V_C signal is below V_{TH}, the BOOST pulses are absent, as can be seen in Figure 2b. Now the DC current activated by the SWON signal alone drives Q4 and this transistor drives Q1 by itself. The absence of a BOOST pulse plus the lack of a second NPN driver results in a much lower slew rate, which aids light load controllability.

A further aid to overall efficiency is provided by the specialized bias regulator circuit, which has a pair of inputs, V_{IN} and V_{CC}. The V_{CC} pin is normally connected to the switching supply output. During start-up conditions, the LT1676/LT1776 power themselves directly from V_{IN}. However, after the switching supply output voltage reaches about 2.9V, the bias regulator uses this supply as its input. Previous generation step-down controller ICs without this provision typically required hundreds of milliwatts of quiescent power when

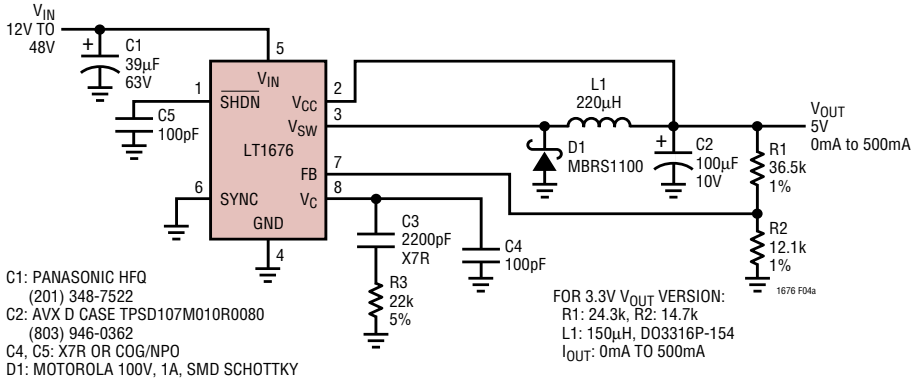


Figure 3a. Minimum component-count application

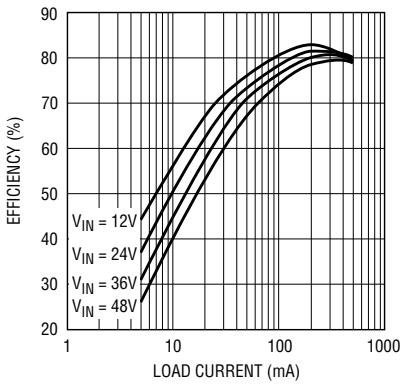
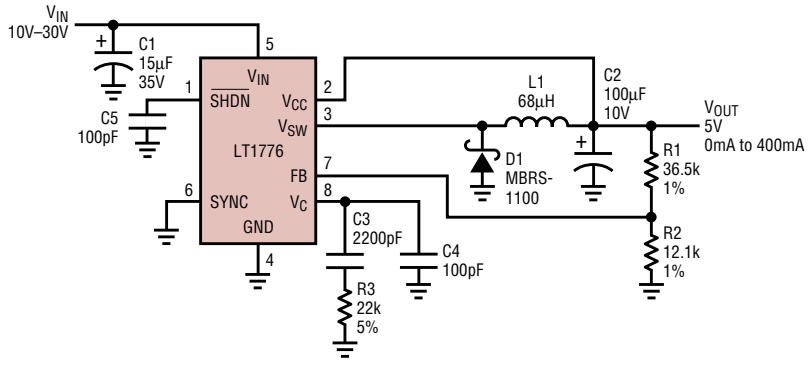


Figure 3b. Efficiency of Figure 3a's circuit



C1: AVX D CASE 15µF 35V
TPSD156M035R0300
(803) 946-0362
C2: AVX D CASE 100µF 10V
TPSD107M010R0080
C3: 2200pF, X7R

C4, C5: 100pF, X7R OR COG/NPO
D1: MOTOROLA 100V, 1A, SMD SCHOTTKY
MBRS1100
(800) 441-2447
L1: COILCRAFT DO1608C-683
(847) 936-6400

FOR 3.3V V_{OUT} VERSION:
I_{OUT}: 0mA TO 500mA
L1: 47µH, DO1608C-473
R1: 24.3k, R2: 14.7k

Figure 4a. Minimum PC board area application

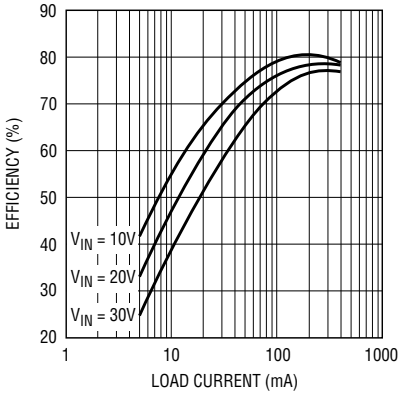
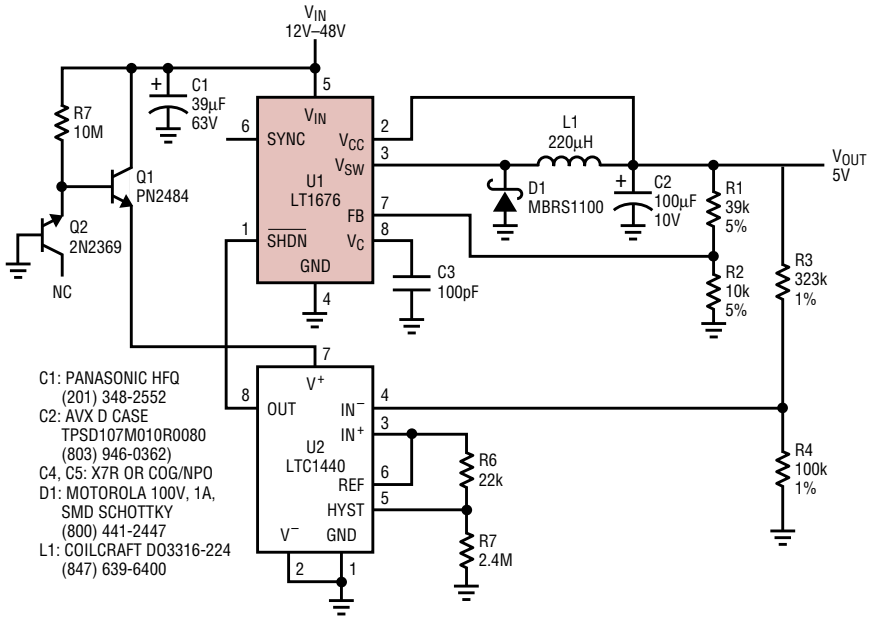


Figure 4b. Efficiency of Figure 4a's circuit

operating at high input voltages. This both degraded efficiency and limited available output current due to internal heating.

Choosing Between the LT1676 and LT1776

As previously mentioned, the LT1676 and LT1776 devices are pin-for-pin compatible and, in fact, nearly identical. The only real difference is in their internal oscillator frequencies, nominally 100kHz for the LT1676 and 200kHz for the LT1776. A user must decide which version is best suited for his or her particular application. Generally, the LT1776 is favored, as its higher switching frequency allows for a lower valued and possibly physically smaller and less costly inductor. However, the higher switching frequency of the LT1776 increases AC switching losses, adversely affecting efficiency and internal power dissipation. In fact, certain combinations of high input voltage and output current may yield unacceptable internal power dissipation and consequent thermal rise. In these cases, the slower switching frequency of the LT1676 may yield acceptable operation. (A more thorough treatment of input voltage vs operating frequency considerations can be found in the LT1776 data sheet.)



C1: PANASONIC HFQ
(201) 348-2552
C2: AVX D CASE
TPSD107M010R0080
(803) 946-0362)
C4, C5: X7R OR COG/NPO
D1: MOTOROLA 100V, 1A,
SMD SCHOTTKY
(800) 441-2447
L1: COILCRAFT DO3316-224
(847) 639-6400

Figure 5a. Burst Mode operation configuration

Applications

Minimum Component-Count Application

Figure 3a shows a basic "minimum component count" application using the LT1676. The circuit produces 5.0V at up to 500mA I_{OUT} with input voltages in the range of 12V to 48V. The typical P_{OUT}/P_{IN} efficiency is shown in Figure 3b. No pulse skipping is observed down to zero external load. (The several milliamperes drawn by the V_{CC} pin acts as a sufficient preload.) As shown, the SHDN and SYNC pins are unused, however either (or both) can be optionally driven by external signals as desired.

Minimum PC Board Area Application

The previous application example used the LT1676 to demonstrate simultaneously the maximum input voltage and output current capability. As such, the input bypass capacitor choice was a high frequency aluminum electrolytic type, rated to

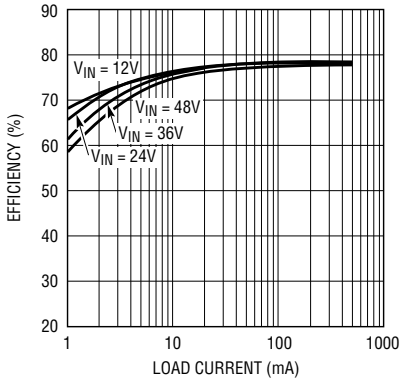


Figure 5b. Efficiency of Figure 5a's circuit

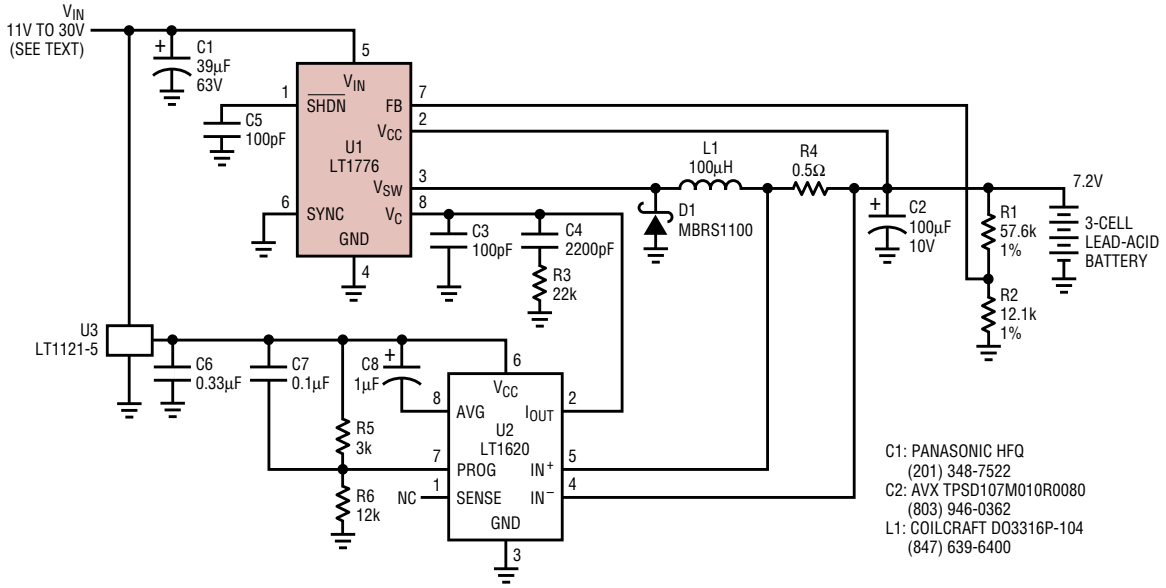


Figure 6a. Wide V_{IN} range, high efficiency battery charger

63V. Also, the 100kHz switching rate of the LT1676 requires an inductor of about 220µH. The DO3316 device size was chosen to support the output current requirements. However, both of these components are physically large.

The application example in Figure 4a shows a circuit that is much smaller physically than the previous minimum component count application. The nominal 200kHz switching frequency of the LT1776 allows the use of a physically smaller 68µH inductor—a Coilcraft DO1608C-683. This inductor will support output current to 400mA at 5V. However, the part is incapable of withstanding an indefinite short circuit to ground. (Momentary shorts of a few seconds or less can still be tolerated.) Additionally, the bulky aluminum electrolytic capacitor previously on V_{IN} has been replaced by a compact 35V-rated tantalum type. The result is a postage-stamp-sized circuit with efficiency as shown in Figure 4b.

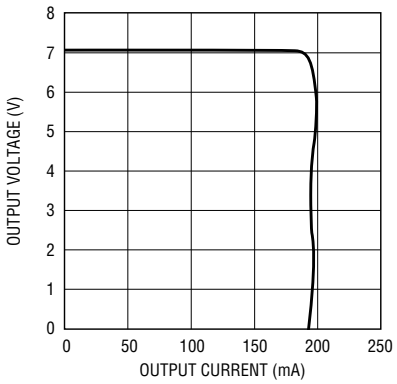


Figure 6b. Battery charger output voltage vs output current for Figure 6a's circuit

Burst Mode Application

The minimum component count application demonstrates that power supply efficiency degrades with lower output load current. This is not surprising, as the LT1676 itself represents a fixed power overhead. A possible way to improve light load efficiency is to use Burst Mode™ operation.

Figure 5a shows the LT1676 configured for Burst Mode operation. Output voltage regulation is now provided in a "bang-bang" digital manner, via comparator U2, an LTC1440. Resistor divider R4/R5 provides a scaled version of the output voltage, which is compared against U2's internal reference. Intentional hysteresis is set by the R6/R7 divider. As the output voltage falls below the regulation range, the LT1676 is turned on. The output voltage rises and, as it climbs above the regulation range, the LT1676 is turned off. Efficiency is maximized as the LT1676 is only powered up while it is providing heavy output current. Figure 5b shows that efficiency is typically maintained at 75% or better down to a load current of 10mA. Even at a load current of 2mA, efficiency is still a respectable 65% to 75% (depending on V_{IN}).

Resistor divider R1/R2 is still present, but does not directly influence output voltage. It is chosen to ensure that the LT1676 delivers high output current throughout the voltage regulation range. Its presence is also required to maintain proper short-circuit protection. Transistors Q1 and Q2 and resistor R7 form a high V_{IN}, low quiescent current voltage regulator to power U2.

Battery Charger Application

Figure 6a shows the LT1776 configured as a constant-current/constant-voltage battery charger. An LT1620 rail-to-rail current sense amplifier (U2) monitors the differential voltage across current sense resistor R4. As this equals and exceeds the voltage across resistor R5 in the R5/R6 divider, the LT1620 responds by sinking current at its I_{OUT} pin. This is connected to the V_C control node of the LT1776 and therefore acts to reduce the amount of power delivered to the load. The overall constant-current/constant-voltage behavior can be seen in Figure 6b.

Target voltage and current limits are independently programmable. The output voltage of 7.2V, which corresponds to the charging voltage of a 3-cell lead-acid battery, is set by the R1/R2 divider and the internal refer-

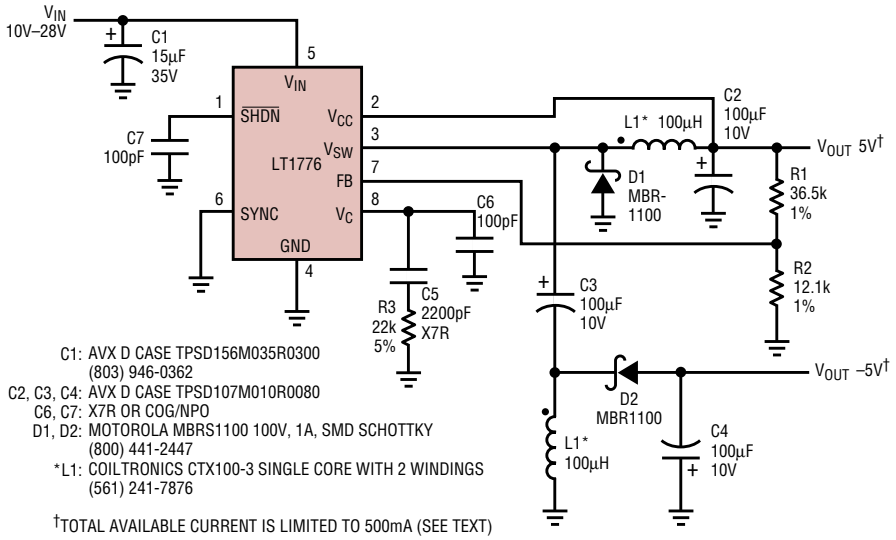


Figure 7. Dual-output SEPIC converter

ence of the LT1776. Output current, presently 200mA, is set by current sense resistor R4 and the R5/R6 divider. (A 16-pin version of the LT1620 that implements end-of-cycle detection is also available. This is useful for implementing lead-acid battery "top-off" charger behavior or the like. See the LT1620 data sheet for further information.)

The circuit as shown accommodates an input voltage range of 11V to 30V. The upper input voltage limit of 30V is determined not by the LT1776, but by the LT1121-5 regulator (U3). (A regulated 5V is required by the LT1620.) This regulator was chosen for its micropower behavior, which helps maintain good overall efficiency. However, the basic catalog part is only rated to 30V. Substitution of the industry standard LM317, for example, extends the allowable input voltage to 40V (or more with the HV version), but its greater quiescent current drain degrades efficiency from that shown.

Dual Output SEPIC Converter

All of the previous applications provide a single positive output voltage. Real world situations often require dual supply voltages. The SEPIC topology (single-ended primary inductance converter) offers a cost-effective way to simultaneously generate a negative voltage with a single piece of magnetics. The circuit in Figure 7 uses an LT1776 to generate both positive and negative 5V. The two inductors shown are actually just two windings on a standard Coiltronics inductor. Capacitor C3 creates the SEPIC topology, which improves regulation and reduces ripple current in L1.

For the best negative supply voltage regulation, this output should have a preload of at least 1% of the maximum positive load. Total available current from both outputs is limited to 500mA. Maximum negative supply current is limited by the positive 5V load. A typical limit is one-half of the positive current, but a more exact calculation includes the input voltage. For this and further details of this topology, see Linear Technology Design Note 100.

Positive-to-Negative Converter

The previous example used a dual inductor to create a pair of output voltages, one positive and the other negative. The positive-to-negative converter topology illustrated in Figure 8 generates a single negative output voltage from a positive input voltage, using just an ordinary inductor. The topology is somewhat similar to the original step-down arrangement, but the inductor is grounded and the LT1776 ground is now referred to the negative output voltage. Note that the integrated circuit must now be rated for the worst case sum of the input voltage plus the absolute value of the output voltage. The relatively high input voltage rating of the LT1676/LT1776 parts along with their good efficiency under such conditions make them an excellent choice for implementing this topology. The circuit as shown converts an input voltage in the range of 10V to 28V to a –5V output. Available output current is 300mA at the worst case V_{IN} of 10V.

The user should exercise caution in modifying this circuit for other applications. The positive-to-negative topology is not as straightforward as the step-down topology. It is actually more like a flyback topology, in that current is delivered to the output in

continued on page 20

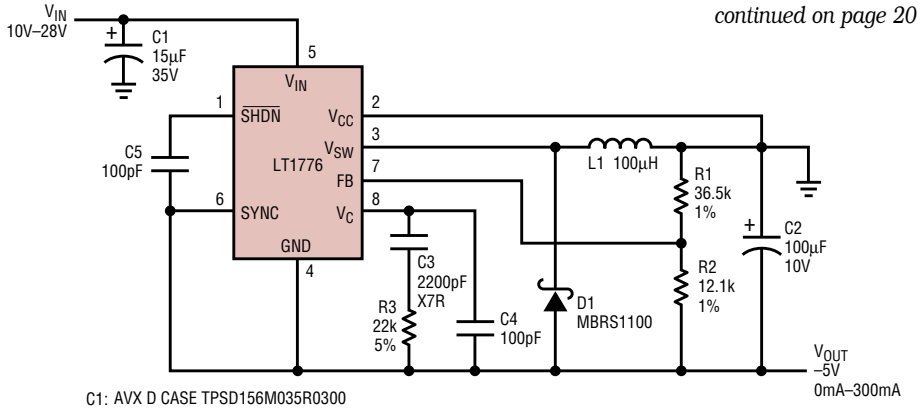


Figure 8. Positive-to-negative converter

A 4.5ns, 4mA, Single-Supply, Dual Comparator Optimized for 3V/5V Operation

by Joseph G. Petrofsky

Introduction

The LT1720 is an UltraFast™ (4.5ns), low power (4mA/comparator), single-supply, dual comparator designed to operate on a single 3V or 5V supply. These comparators feature internal hysteresis, making them easy to use, even with slowly moving input signals. The LT1720 is fabricated in Linear Technology's 6GHz complementary bipolar process, resulting in unprecedented speed for its low power consumption. Table 1 summarizes the LT1720's performance specifications.

The LT1720 is offered in SO-8, with just three pins per comparator plus power and ground. For a full-featured, 7ns, single-supply comparator with dual complementary outputs and internal latch, the LT1394 is available from this same high speed process.

These fast, small, low power comparators are versatile building blocks for a variety of high speed, single-supply applications, such as clock generators, window comparators, timing skew generators, coincidence detectors and pulse stretchers.

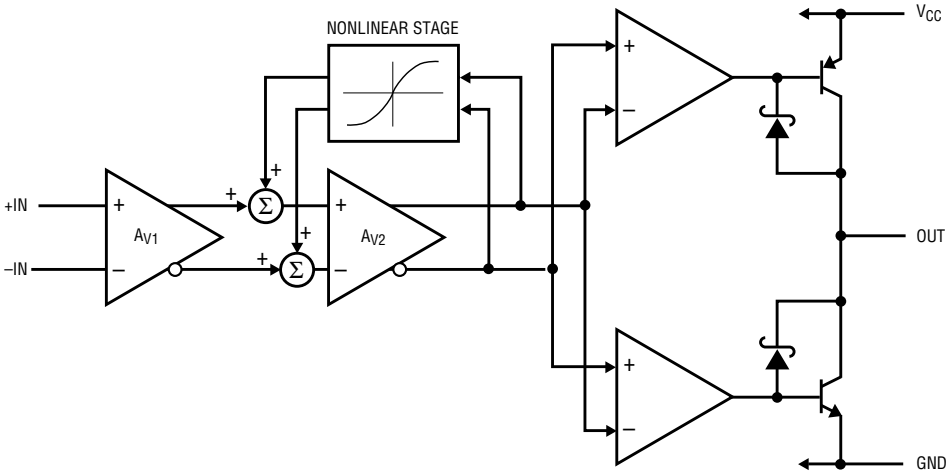


Figure 1. LT1720 block diagram

Circuit Description

The block diagram of one comparator in the LT1720 is shown in Figure 1. There are differential inputs (+IN/–IN), an output (OUT), a single positive supply (V_{CC}) and ground (GND). The two comparators are completely independent, sharing only the power and ground pins. The circuit topology consists of a differential input stage, a gain stage with hysteresis and a complementary common-emitter output stage. All of the internal signal paths utilize low voltage swings for high speed at low power.

The input stage topology maximizes the input dynamic range available without requiring the power, complexity and die area of two complete input stages such as are found in rail-to-rail input comparators. With a 2.7V supply, the LT1720 still has a respectable 1.6V of input common mode range. The differential input voltage range is rail-to-rail, without the large input currents found in competing devices. The input stage also features phase reversal protection to prevent false outputs when the inputs are driven below the –100mV common mode voltage limit.

The internal hysteresis is implemented by positive, nonlinear feedback around a second gain stage. Until this point, the signal path has been entirely differential. The signal path is then split into two drive signals for the upper and lower output transistors. The output transistors are connected common emitter for rail-to-rail output operation. The

Table 1. Typical LT1720 specifications, T_A = 25°C

Parameter	Conditions	Value
Propagation Delay	Overdrive = 20mV	4.5ns
Propagation Delay	Overdrive = 5mV	7ns
Supply Current	V_{CC} = 5V	4mA per Comparator
Supply Voltage	Full Temperature Range Limits	2.7V to 6V
Input Voltage Range	Full Temperature Range Limits	–0.1V to (V_{CC} – 1.2V)
Input Offset Voltage	V_{CC} = 5V, V_{CM} = 1V	1mV
Input-Referred Hysteresis	V_{CC} = 5V, V_{CM} = 1V	3.5mV
Output Voltage (Low)	I_{SINK} = 10mA	0.4V Max
Output Voltage (High)	I_{SOURCE} = 4mA	(V_{CC} – 0.4V) Min

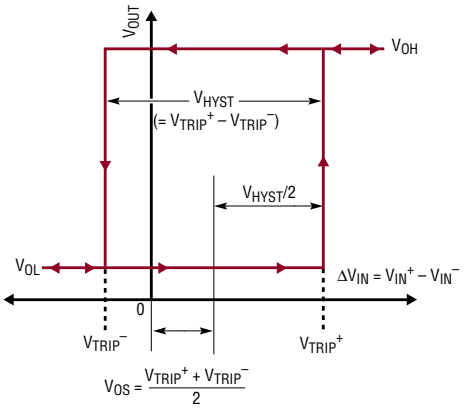


Figure 2. Hysteresis I/O characteristics

Schottky clamps limit the output voltages at about 300mV from the rail, not quite the 50mV or 15mV of Linear Technology's rail-to-rail amplifiers and other products. But the output of a comparator is digital, and this output stage can drive TTL or CMOS directly. It can also drive a host of other loads, as will be demonstrated in the applications below.

The bias conditions and signal swings in the output stages are designed to turn their respective output transistors off faster than on. This nearly eliminates the surge of current from V_{CC} to ground that occurs at transitions, keeping the power consumption low even with high output-toggle frequencies. In fact, the internal-frequency-dependent current drain is the equivalent of putting just 15pF on the output. The low surge current also helps keep the LT1720 well behaved in high speed applications.

Internal Hysteresis

The LT1720 includes internal hysteresis, eliminating the linear region where high speed comparators are most temperamental. The input-output transfer characteristic is illustrated in Figure 2, which shows the definitions of V_{OS} and V_{HYST} based upon the two measurable trip points. The 3.5mV (typical) hysteresis band makes the LT1720 well behaved, even with slowly moving inputs.

The exact amount of hysteresis will vary from unit-to-unit; the LT1720 specifications include both upper and lower limits that are guaranteed over temperature. The hysteresis will also vary slightly with changes in supply voltage and common mode voltage. If a comparator is used to detect a threshold crossing in one direction only, only that trip point is significant. Therefore, a stable offset voltage with an unpredictable level of hysteresis, as seen in many competing comparators, is useless. The LT1720 is many times better than prior comparators in this regard. Figure 3 shows a typical LT1720's input voltages vs supply voltages. The V_{OS} shift is only 320µV, corresponding to a typical PSRR of 80dB.

Speed Limits

The LT1720 comparators are intended for high speed applications, where it is important to understand a few limitations. These limitations can roughly be divided into three categories: input speed limits, output speed limits and internal speed limits.

There are no significant input speed limits except the shunt capacitance of the input nodes. If the 2pF typical input nodes are driven, the LT1720 will respond.

The output speed is constrained by the slew currents available from the output transistors. To maintain low power quiescent operation, the LT1720 output transistors are sized to deliver 25mA–45mA typical slew currents. This is sufficient to drive small capacitive loads and logic gate inputs at extremely high speeds. But the slew rate will slow dramatically

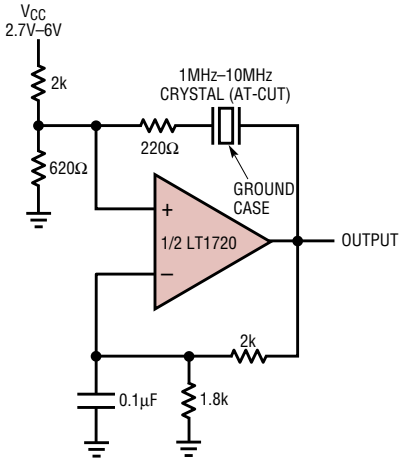


Figure 4. Simple 1MHz–10MHz crystal oscillator

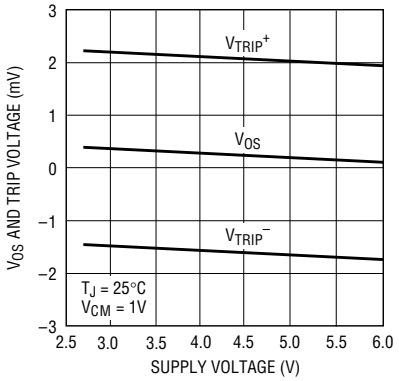


Figure 3. The LT1720's hysteresis is insensitive to supply-voltage variations.

with heavy capacitive loads. Because the propagation delay (t_{PD}) definition ends at the time the output voltage is halfway between the supplies, the fixed slew current actually makes the LT1720 faster at 3V than 5V with 20mV of input overdrive.

The internal speed limits manifest themselves as dispersion. All comparators have some degree of dispersion, defined as a change in propagation delay vs input overdrive. The propagation delay of the LT1720 will vary with overdrive, from a typical of 4.5ns at 20mV overdrive to 7ns at 5mV overdrive (typical). The LT1720's primary source of dispersion is the hysteresis stage. As a change of polarity arrives at the gain stage, the positive feedback of the hysteresis stage subtracts from the overdrive available. Only when enough time has elapsed for a signal to propagate forward through the gain stage, backwards through the hysteresis stage and forward through the gain stage again, will the output stage receive the same level of overdrive that it would have received in the absence of hysteresis.

With 5mV of overdrive, the LT1720 is faster with a 5V supply than with a 3V supply, the opposite of what is true with 20mV overdrive. This is due to the internal speed limit, because the gain stage is faster at 5V than 3V due primarily to the reduced junction capacitances with higher reverse voltage bias.

In many applications, as shown in the following examples, there is plenty of input overdrive. Even in applica-

tions providing low levels of overdrive, the LT1720 is fast enough that the absolute dispersion of 2.5ns (= 7 – 4.5) is small enough to ignore.

The gain and hysteresis stage of the LT1720 is simple, short and high speed to minimize dispersion. This internal "self-latch" can be usefully exploited in many applications because it occurs early in the signal chain, in a low power, fully differential stage. It is therefore highly immune to disturbances from other parts of the circuit, either in the same comparator, on the supply lines or from the other comparator in the same package. Once a high speed signal trips the hysteresis, the output will respond, after a fixed propagation delay, without regard to these external influences that can cause trouble in nonhysteretic comparators.

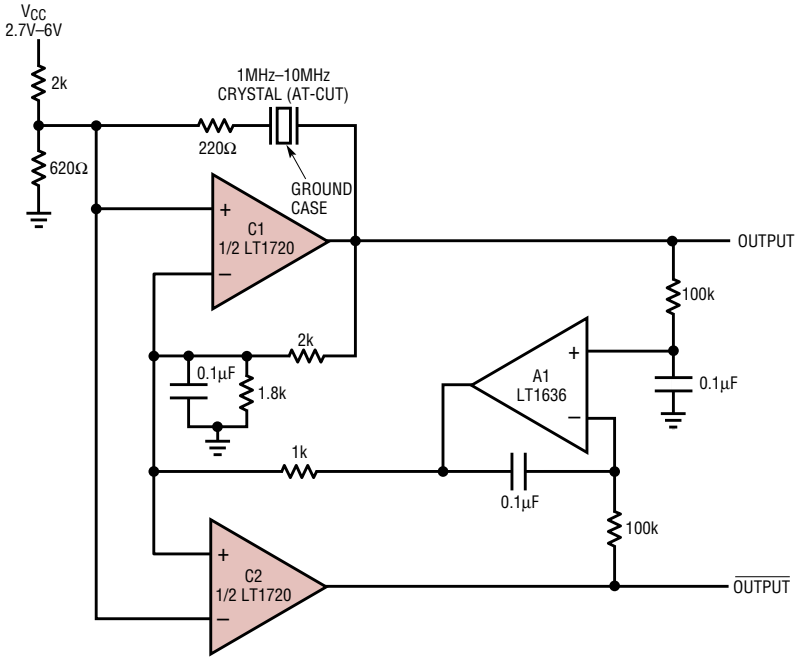


Figure 5. Crystal oscillator with complementary outputs and 50% duty cycle

Applications

Crystal Oscillators

Figure 4 shows a simple crystal oscillator using one half of an LT1720. The 2k–620Ω resistor pair set a bias point at the comparator's noninverting input. The 2k–1.8k–0.1µF path sets the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. Although the LT1720 will give the correct logic output when one input is outside the common mode range, additional delays may occur when it is so operated, opening the possibility of spurious operating modes. Therefore, the DC bias voltages at the inputs are set near the center of the LT1720's common mode range and the 220Ω resistor attenuates the feedback to the noninverting input. The circuit will operate with any AT-cut crystal from 1MHz to 10MHz over a 2.7V to 6V supply range.

The output duty cycle for the circuit of Figure 4 is roughly 50% but it is affected by resistor tolerances and, to a lesser extent, by comparator offsets and timings.

The circuit of Figure 5 creates a pair of complementary outputs with a forced 50% duty cycle. Crystals are narrow-band elements, so the feedback to the noninverting input is a filtered analog version of the square wave output. Changing the noninverting reference level can therefore vary the duty cycle. C1 operates as in the previous example, whereas C2 creates a complementary output by comparing the same two nodes with the opposite input polarity. A1 compares band-limited versions of the outputs and biases C1's negative input. C1's only degree of freedom to respond is variation of pulse width; hence the outputs are forced to 50% duty cycle. This circuit works well because of the two matched delays and rail-to-rail style outputs.

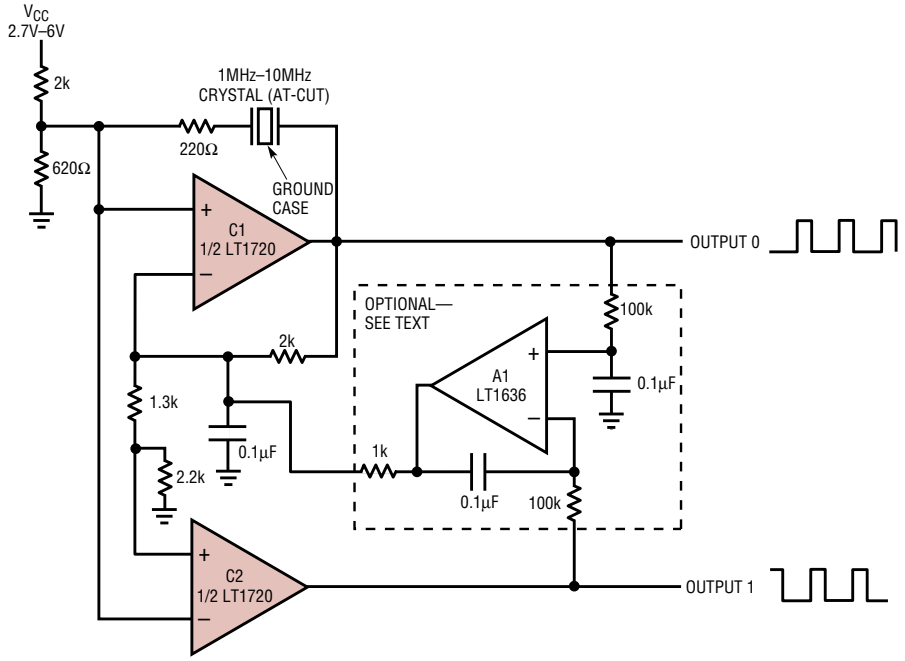


Figure 6. Crystal-based nonoverlapping 10MHz clock generator

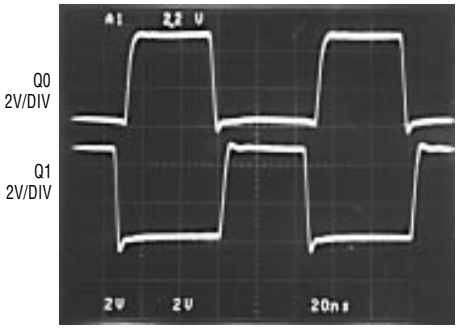


Figure 7, Nonoverlapping outputs of Figure 6's circuit

The circuit in Figure 6 shows a crystal oscillator circuit that generates two nonoverlapping clocks by making full use of the two independent comparators of the LT1720. C1 oscillates as before, but with a lower reference level, C2's output will toggle at different times. The resistors set the degree of separation between the output's high pulses. With the values shown, each output has a 44% high and 56% low duty cycle, sufficient to allow 2ns between the high pulses where both are at logic low. Figure 7 shows the two outputs.

The optional A1 feedback network shown can be used to force identical output duty. Because the reference level set for C2 is lower than that set for C1, the steady state duty cycles will be 44% rather than 50%. Note, though, that the addition of this network only adjusts the percentage of time each output is high to be the same, which can be important in switching circuits requiring identical settling times. It cannot adjust the relative phases between the two outputs to be exactly 180° apart because the signal at the input node driven by the crystal is not an exact sinusoid.

Timing Skews

For a number of reasons, the LT1720 is an excellent choice for applications requiring differential timing skew. The two comparators in a single package are inherently well matched, with just 300ps Δt_{PD} typical. Monolithic construction keeps the delays well matched vs supply voltage and temperature. Crosstalk between the comparators, usually a disadvantage in monolithic duals, has minimal effect on the LT1720 timing due to the internal hysteresis, as discussed earlier.

The circuits of Figure 8 show basic building blocks for differential timing skews. The 2.5k resistance interacts with the 2pF typical input capacitance to create at least ±4ns delay, controlled by the potentiometer setting. A differential and a single-ended version are shown. In the differential configuration, the output edges can be smoothly scrolled through $\Delta t = 0$ with negligible interaction.

Fast Waveform Sampler

Figure 9 uses a diode-bridge-type switch for clean, fast waveform sampling. The diode bridge, because of its inherent symmetry, provides lower AC errors than other semiconductor-based switching technologies. This circuit features 20dB of gain, 10MHz full power bandwidth and 100µV/°C baseline uncertainty. Switching delay is less than 15ns and the minimum sampling window width for full power response is 30ns.

The input waveform is presented to the diode bridge switch, the output of which feeds the LT1227 wideband amplifier. The LT1720 comparators, triggered by the sample command, generate phase-opposed outputs. These signals are level shifted by the transistors, providing complementary bipolar drive to switch the bridge. A skew compensation trim ensures bridge-drive signal simultaneity within 1ns. The AC balance corrects for parasitic capacitive bridge imbalances. A DC balance adjustment trims bridge offset.

The trim sequence involves grounding the input via 50Ω and applying a 100kHz sample command. The DC balance is adjusted for minimal bridge ON vs OFF variation at the output. The skew compensation and AC balance adjustments are then optimized for minimum AC disturbance in the output. Finally, unground the input and the circuit is ready for use.

Coincidence Detector

High speed comparators are especially suited for interfacing pulse-output transducers, such as particle detectors, to logic circuitry. The matched

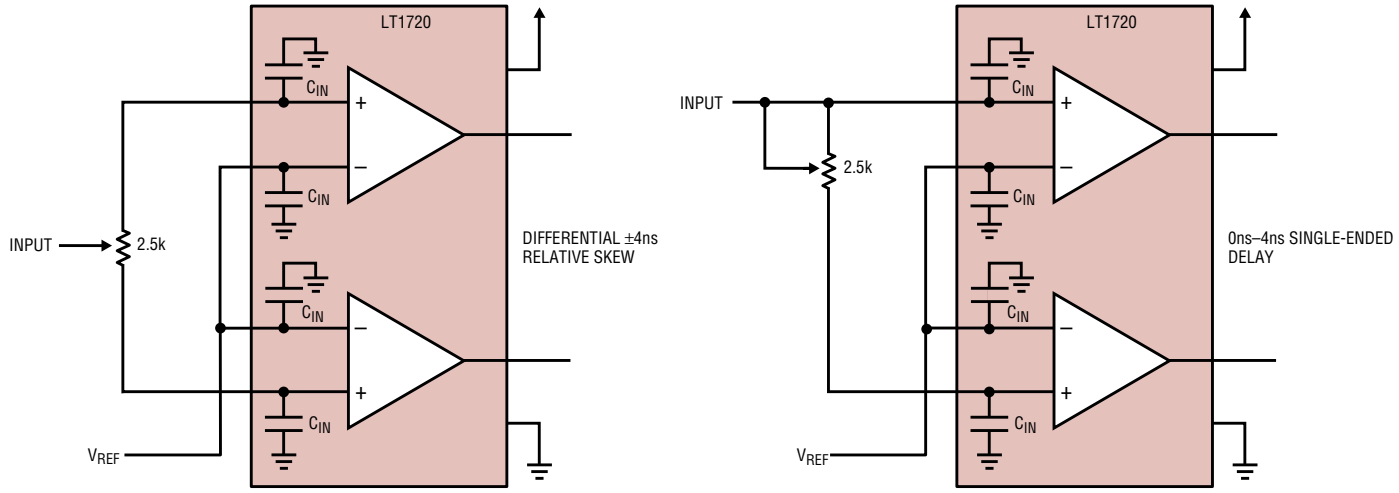


Figure 8. Timing-skew generation is easy with the LT1720.

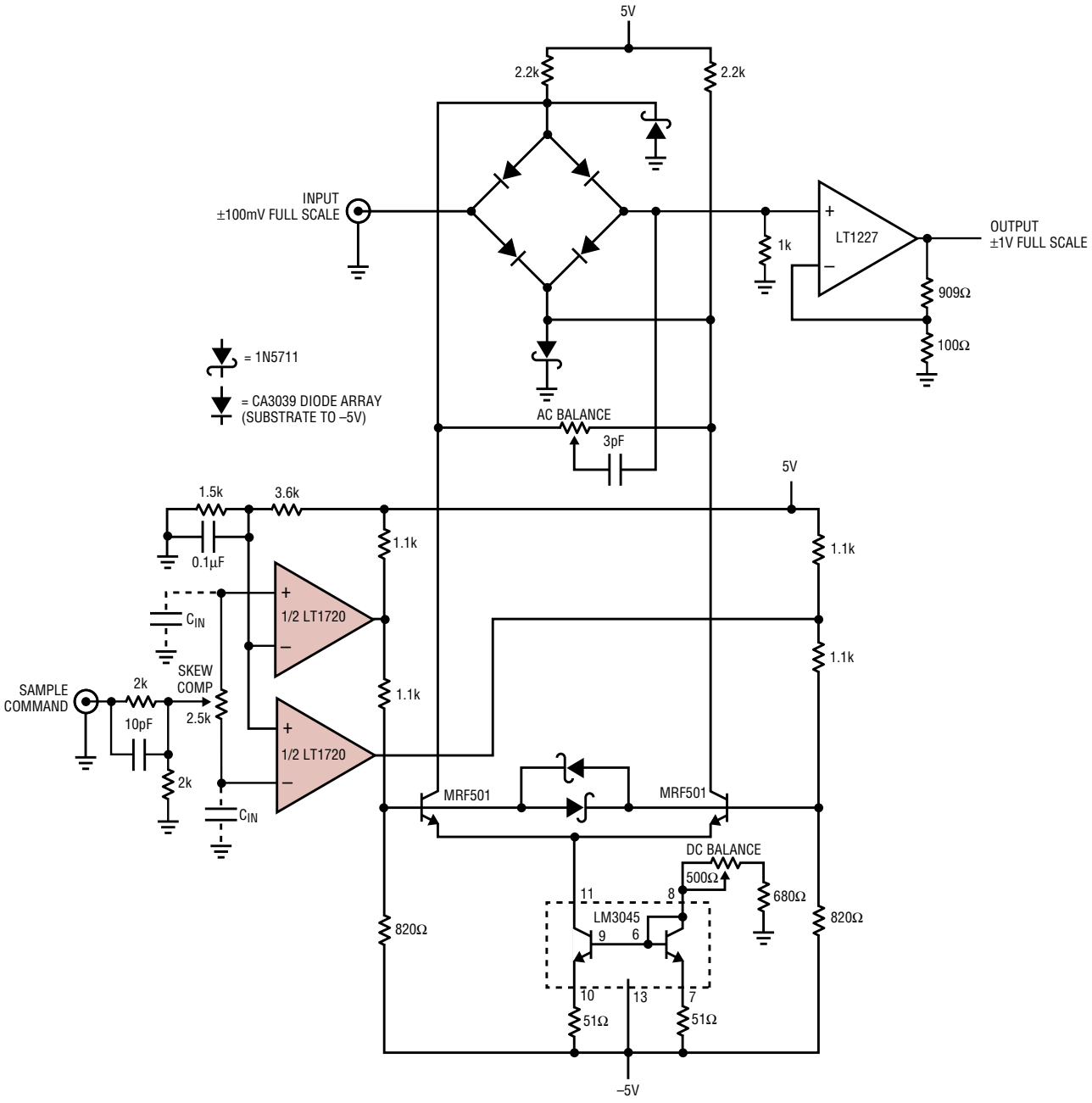


Figure 9. Fast waveform sampler using the LT1720 for timing-skew compensation

delays of a monolithic dual are well suited for those cases where the coincidence of two pulses needs to be detected. The circuit of Figure 10 is a coincidence detector that uses an LT1720 and discrete components as a fast AND gate.

The reference level is set to 1V, an arbitrary threshold. Only when both input signals exceed this will a coincidence be detected. The Schottky diodes from the comparator outputs to the base of the MRF-501 form the AND gate, while the other two Schottkys provide for fast turn-off. A logic AND gate could instead be used, but would add considerably more delay than the 300psec contributed by this discrete stage.

This circuit can detect coincident pulses as narrow as 2.5ns. For narrower pulses, the output will degrade gracefully, responding, but with narrow pulses that don't rise all the way to high before starting to fall. The decision delay is 4.5ns with input signals 50mV or more above the reference level. This circuit creates a TTL compatible output but it can typically drive CMOS as well.

Pulse Stretcher

For detecting short pulses from a single sensor, a pulse stretcher is often required. The circuit of Figure 11 acts as a one-shot, stretching the width of an incoming pulse to a consistent 100ns. Unlike a logic one-shot, this LT1720-based circuit requires only 100pV-s of stimulus to trigger.

The circuit works as follows: Comparator C1 functions as a threshold

detector, whereas comparator C2 is configured as a one-shot. The first comparator is prebiased with a threshold of 8mV to overcome comparator and system offsets and establish a low output in the absence of an input signal. An input pulse sends the output of C1 high, which in turn latches C2's output high. The output of C2 is fed back to the input of the first comparator, causing regeneration and latching both outputs high. Timing capacitor C now begins charging through R and, at the end of 100ns, C2 resets low. The output of C1 also goes low, latching both outputs low. A new pulse at the input of C1 can now restart the process. Timing capacitor C can be increased without limit for longer output pulses.

This circuit has an ultimate sensitivity of better than 14mV with 5ns–10ns input pulses. It can even detect an avalanche generated test pulse of just 1ns duration with sensitivity better than 100mV.[1] It can detect short events better than the coincidence detector above because the one-shot is configured to catch just 100mV of upward movement from C1's V_{OL}, whereas the coincidence detector's 2.5ns specification is based on a full, legitimate logic high.

Conclusion

The new LT1720 dual 4.5ns single-supply comparators feature high speeds and low power consumption. They are versatile and easy-to-use building blocks for a wide variety of system design challenges.

[1] See Linear Technology Application Note 47, Appendix B. This circuit can detect the output of the pulse generator described after 40dB of attenuation.

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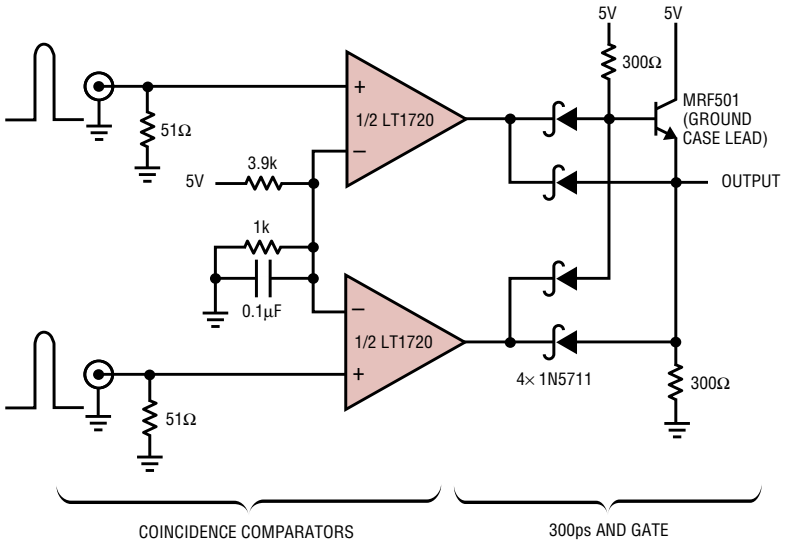

Figure 10. A 2.5ns coincidence detector

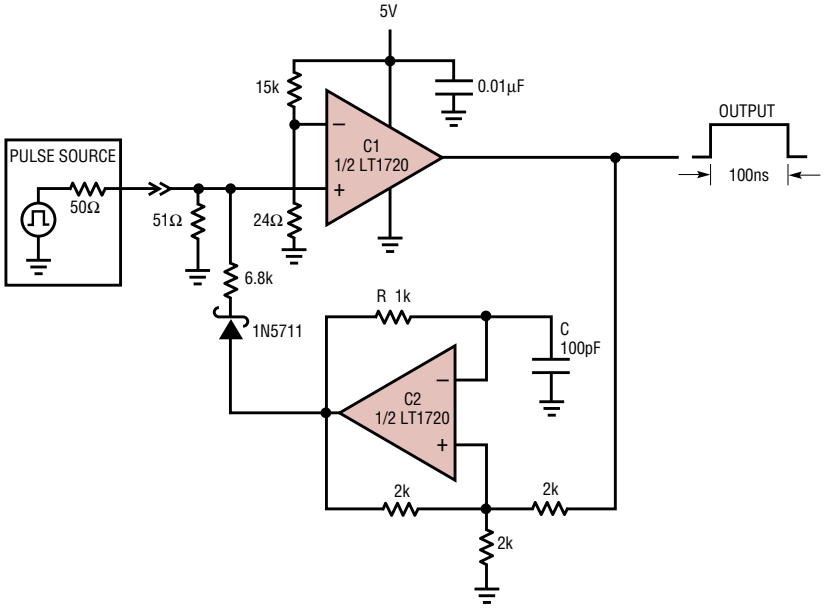

Figure 11. A 1ns pulse stretcher

250MHz RGB Video Multiplexer in Space-Saving Package Drives Cables, Switches Pixels at 100MHz

by John Wright and Frank Cox

Introduction

One of the first products from LTC's new proprietary high speed bipolar process is a 250MHz RGB (red, green, blue) multiplexer that is optimized for switching speed and makes excellent use of the new complementary 6GHz transistors. This new MUX, the LT1675, is designed for pixel switching in video graphics and for RGB routing. It is configured with three SPDT (single pole, double throw) RGB video switches and three current feedback amplifiers for direct driving of cables.

The new RGB MUX is similar to the LT1203/LT1205 video switches combined with the LT1260 triple CFA, but with greatly enhanced performance in far less space. The boost over the older configuration is a factor of five in switching speed and a factor of 2.5 in bandwidth, while the PCB footprint is reduced by more than five. This "juiced" performance is accomplished with one-third less supply current than required by the equivalent multichip design.

Dense Process Yields Big Performance from Tiny PC Board Space

One advantage of the dense, high speed bipolar process is that it results in a reduced die size for the LT1675, even though it has well over 300 active devices. The benefit to the user is that the LT1675 comes in a small 16-pin SSOP package, which is the same size as an SO-8. To enhance the small PC board theme, the LT1675 is configured for a fixed gain of two, eliminating six external gain setting resistors. The fixed gain of two in the CFA is ideal for driving double terminated 50Ω or 75Ω cables. Additionally, stray PCB capacitance on the sensitive feedback node is no longer a problem. Figure 1 shows a typical application switching between two RGB sources and driving 75Ω cables. In contrast, some competitive solutions are housed in bulky 24-pin, wide-SO packages and draw significantly more supply current.

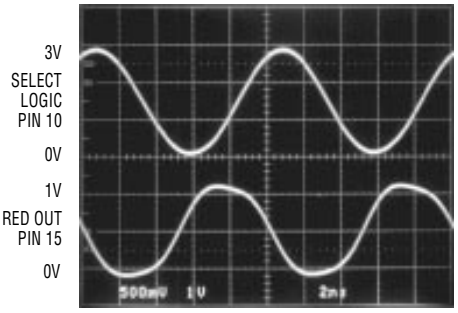

Figure 2. Select pin switches inputs at 100MHz. RED 1 = 0V, RED 2 = 1V, R_L = 100Ω, 10pF scope probe; measured between 50Ω back termination and 50Ω load

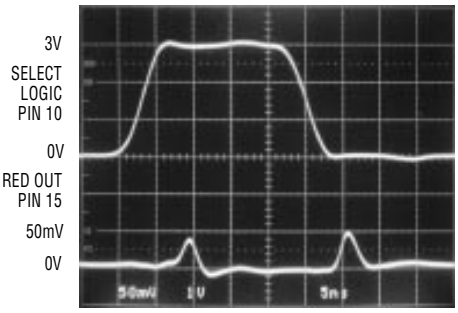

Figure 3. Input-referred switching transient. R_L = 150Ω, 10pF scope probe

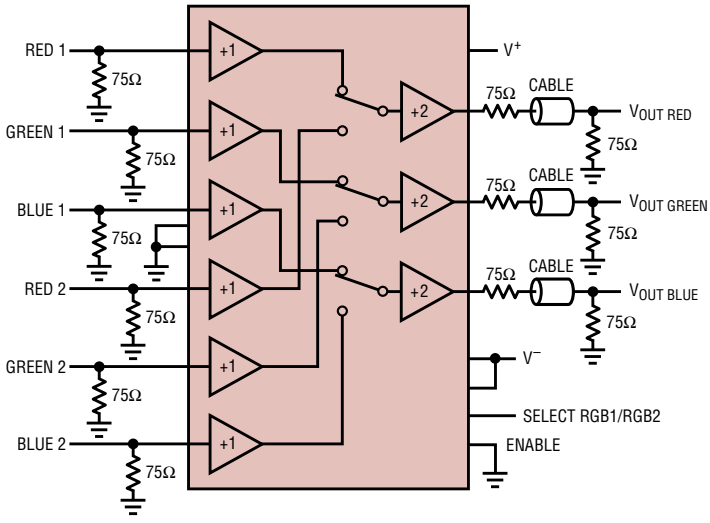

Figure 1. LT1675 typical application: switching between two RGB sources and driving three cables

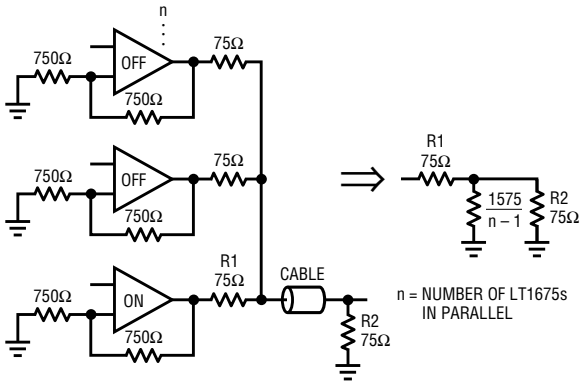

Figure 4. Each off channel loads the cable termination with the 1575Ω.

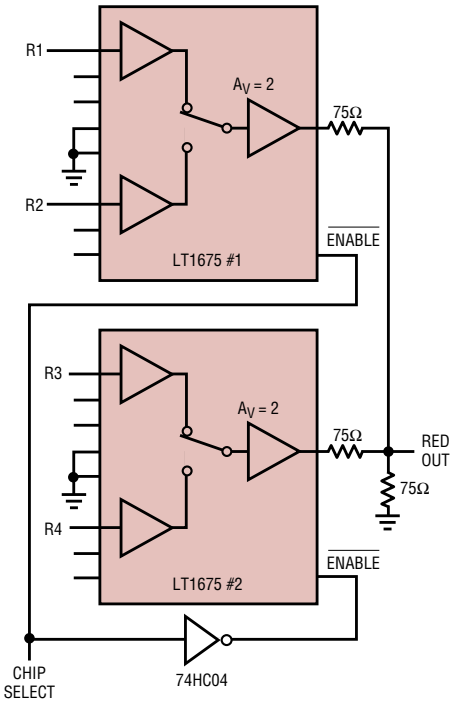

Figure 5. Two LT1675s build a 4-input RGB router.

The LT1675's internal switches change state in less than 1ns but the output of the MUX switches in 2.5ns. This increased time is due to the finite bandwidth of the current feedback amplifier that drives the cable. To toggle at 100MHz, as shown in Figure 2, implies a pixel width of 5ns; accomplishing this requires a slew rate in excess of 1000V/µs. In Figure 2, the Select pin (pin 10) is driven from a sine wave generator, since only crossings of the logic threshold are required.

The fast current steering break-before-make SPDT tee switches minimize switching glitches. The switching transients of Figure 3, measured between the 75Ω back termination and the 75Ω load, show what the monitor receives. The glitch is only 50mV$_{p-p}$, the duration is only 5ns and nature of this transient is small and fast enough to not be visible even on quality graphics terminals. Additionally, the break-before-make SPDT switch is open before the alternate channel is connected, which means there is no input feedthrough or crosstalk during switching.

Expanding Inputs Does Not Increase Power Dissipation

In video routing applications, where the ultimate in speed is not mandatory, as it is in pixel switching, it is possible to expand the number of MUX inputs by shorting the LT1675 outputs together and switching with the $\overline{\text{ENABLE}}$ pins. This technique does not increase the power dissipation because LT1675s draw virtually zero current when disabled. The internal gain-set resistors have a nominal value of 750Ω and cause a 1500Ω shunt across the 75Ω cable termination. Figure 4 shows schematically the effect of expanding the number of inputs. The effect of this loading is to cause a gain error that can be calculated by the following formula:

$$\text{GAIN ERROR (dB)} = 6\text{dB} + 20\log\left(\frac{\frac{1575\Omega}{n-1}\,\|\,75\Omega}{75\Omega + \frac{1575\Omega}{n-1}\,\|\,75\Omega}\right)\text{dB}$$

where n is the total number of LT1675s.

For example, using ten LT1675s (20 red, 20 green, 20 blue) the gain error is only –1.7dB per channel.

Figure 5 shows a 4-input RGB router. The response from red 1 input to red output is shown in Figure 6, for a 25MHz square wave with Chip Select = 0V. In this example, the gain error is just –0.23dB. The response to toggling between IC1 and IC2 with Chip Select is shown in Figure 7. In this case red 1 input is connected to 0V, and red 3 is connected to an uncorrelated sine wave.

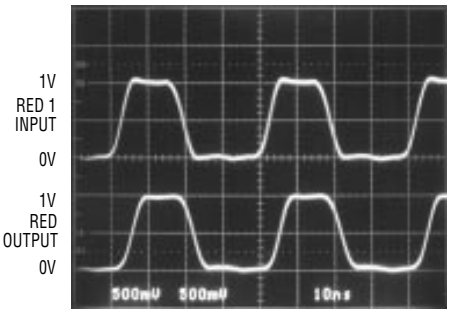

Figure 6. Square wave response: chip select = 0V, IC 2 disabled

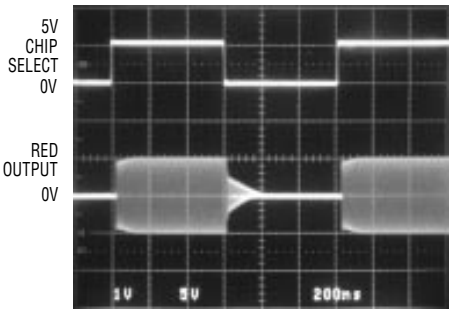

Figure 7. Toggling the 4-input router: Red 1 input = 0V; Red 3 input = uncorrelated sine wave

continued on page 20

Table 1. LT1675 performance, V_S = ±5V

Parameter	Conditions	Typical Values
–3dB Bandwidth	R_L = 150Ω	250MHz
0.1dB Gain Flatness	R_L = 150Ω	70MHz
Crosstalk	Between Active Channels at 10MHz	–60dB
Slew Rate	R_L = 150Ω	1100V/µs
Differential Gain	R_L = 150Ω	0.07%
Differential Phase	R_L = 150Ω	0.05°
Channel Select Time	R_L = 150Ω,V_{IN} = 1V	2.5ns
Enable Time	R_L = 150Ω	10ns
Output Voltage Swing	R_L = 150Ω	±3V
Gain Error	R_L = 150Ω,V_{IN} = ±1V	4%
Output Offset Voltage		20mV
Supply Current	All Three Channels Active	30mA
Supply Current Disabled		1µA

LT1468: An Operational Amplifier for Fast, 16-Bit Systems

by George Feliz

Introduction

The LT1468 is a single operational amplifier that has been optimized for accuracy and speed in 16-bit systems. Operating from ±15V supplies, the LT1468 in a gain of –1 configuration will settle in 900ns to 150µV for a 10V step. The LT1468 also features the excellent DC specifications required for 16-bit designs. Input offset voltage is 75µV max, input bias current is 10nA maximum for the inverting input and 40nA maximum for the noninverting input and DC gain is 1V/µV minimum. The LT1468 specifications are summarized in Table 1. Two key applications that illustrate its use are current-to-voltage (I/V) conversion following a fast, 16-bit current output digital-to-analog converter (DAC), such as LTC1597 (Figure 1), and buffering the input of an analog-to-digital converter (ADC), such as the 333ksps LTC1604 (Figure 2). Both applications will be discussed in detail to highlight the LT1468 design requirements and trade-offs.

16-Bit DAC Current-to-Voltage Converter with 1.7µs Settling Time

The key AC specification of the circuit of Figure 1 is settling time as it limits the DAC update rate. The settling time measurement is an exceptionally difficult problem that has been ably addressed by Jim Williams, beginning in the August 1998 issue and concluding in this issue of *Linear Technology* magazine and, in greater detail, in Linear Technology Application Note 74. Minimizing settling time is limited by the need to null the DAC output capacitance, which varies from 70pF to 115pF, depending on code. This capacitance at the amplifier input combines with the feedback resistor to form a zero in the closed-loop frequency response in the vicinity of 200kHz–400kHz. Without a feedback capacitor, the circuit will oscillate. The choice of 20pF stabilizes the circuit by adding a pole at 1.3MHz to limit the frequency peaking and is chosen to optimize settling time. The settling time to 16-bit accuracy is theoretically bounded by 11.1 time constants set by the 6kΩ and 20pF. Figure 1's circuit settles in 1.7µs to 150µV for a 10V step. This compares favorably with the 1.33µs theoretical limit and is the best result obtainable with a wide variety of LTC and competitive amplifiers. This excellent settling requires the amplifier to be free of thermal tails in its settling behavior.

The LTC1597 current output DAC is specified with a 10V reference input. The LSB is 25.4nA, which becomes 153µV after conversion by the LT1468, and the full-scale output is 1.67mA, which corresponds to 10V at the amplifier output. The zero-scale offset contribution of the LT1468 is the input offset voltage and the inverting input current flowing through the 6k feedback resistor. This worst-case total of 135µV is less than one LSB. At full-scale there is an insignificant additional 10µV of error due to the 1V/µV minimum gain of the amplifier. The low input offset of the amplifier ensures negligible degradation of the DAC's outstanding linearity specifications.

With its low 5nV/√Hz input voltage noise and 0.6pA/√Hz input current noise, the LT1468 contributes only an additional 23% to the DAC output noise voltage. As with any precision application, and particularly with wide bandwidth amplifiers, the noise bandwidth should be minimized with an external filter to maximize resolution.

Table 1. LT1486 key specifications

Input Offset Voltage	75µV Max
Inverting Input Bias Current	10nA Max
Noninverting Input Bias Current	40nA Max
DC Gain	1V/µV Min
CMRR	96dB Min
Input Noise Voltage	5nV/√Hz
Input Noise Current	0.6pA/√Hz
Gain Bandwidth	90MHz
Slew Rate	22V/µs
THD for $10V_{P-P}$, 100kHz	–96.5dB
DAC Settling Time to 150µV, 10V Step (Figure 1's Circuit)	1.7µs
A_V = –1 Settling Time to 150µV, 10V Step	900ns
Supply Current, V_S = ±15V	5.2mA Max

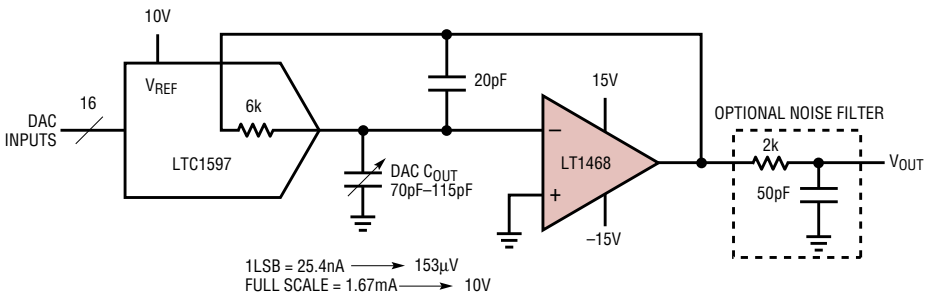

Figure 1. 16-bit DAC I/V converter with 1.7µs settling time

ADC Buffer

The important amplifier specifications for an analog-to-digital converter buffer application (Figure 2) are low noise and low distortion. The LTC1604 16-bit ADC signal-to-noise ratio (SNR)

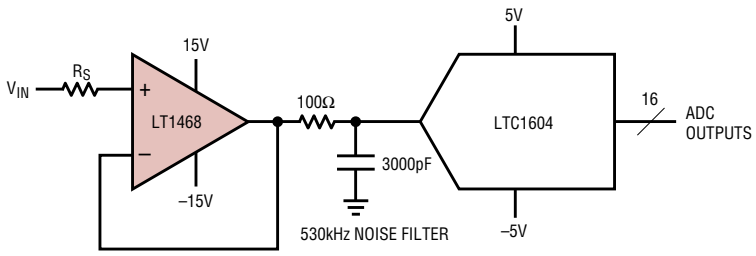

Figure 2. ADC buffer

of 90dB implies 56µV_{RMS} noise at the input. The noise for the amplifier, 100Ω/3000pF filter and a high value 10kΩ source is 15µV_{RMS}, which degrades the SNR by only 0.3dB. The LTC1604 total harmonic distortion (THD) is a low –94dB at 100kHz. The buffer/filter combination alone has 2nd and 3rd harmonic distortion better than –100dB for a 5V_{P-P}, 100kHz input, so it does not degrade the AC performance of the ADC.

The buffer also drives the ADC from a low source impedance. Without a buffer, the LTC1604 acquisition time increases with increasing source resistance above 1k and therefore the maximum sampling rate must be reduced. With the low noise, low distortion LT1468 buffer, the ADC can be driven at maximum speed from higher source resistances without sacrificing AC performance.

The DC requirements for the ADC buffer are relatively modest. The input offset voltage, CMRR (96dB minimum) and noninverting input bias current through the source resistance, R_S, affect the DC accuracy, but these errors are an insignificant fraction of the ADC offset and full-scale errors.

Circuit Description

A simplified schematic of LT1468 is shown in Figure 3. The circuit is a single, folded-cascode gain stage for fast settling and high bandwidth. The inputs are PNP transistors Q1 and Q2 with bias current cancellation from current source I7–Q12 to match Q1 and Q2, and the current mirror composed of Q13, Q14 and Q15. I7 is trimmed to minimize the inverting input current (critical for errors in DAC I/V circuits). The input devices are protected by 100Ω resistors and back-to-back diodes D1 and D2. The collectors of Q1 and Q2 are loaded by current sources I3 and I4 and the emitters of cascode transistors Q3 and Q4. I3 and I4 are trimmed to null the input offset voltage.

The mirror formed by Q5 and Q6 performs differential-to-single ended conversion into the high gain node at the collectors of Q4 and Q6. To increase the gain of this single stage,

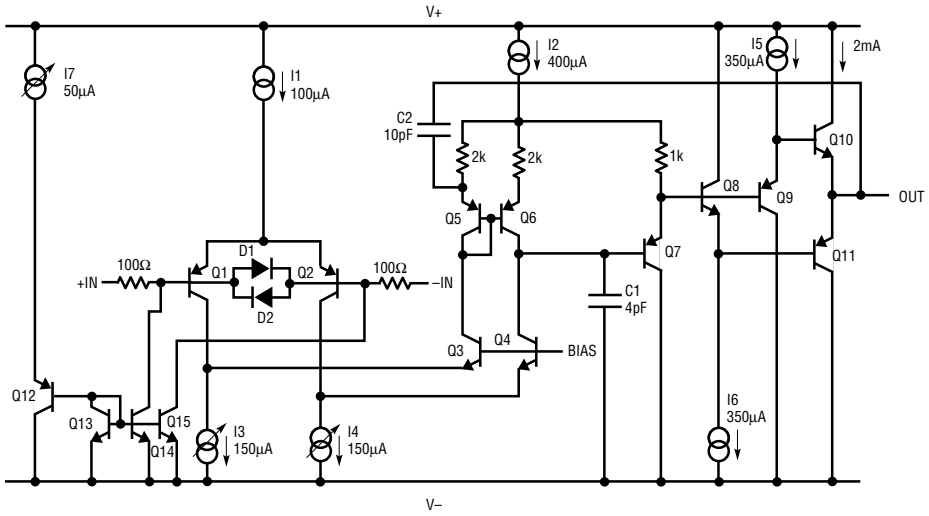

Figure 3. LT1468 simplified schematic

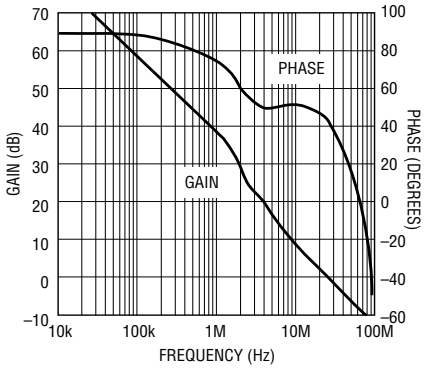

Figure 4. LT1468 gain and phase vs frequency

the Q5–Q6 mirror is bootstrapped by follower Q7 and current source I2 so that the mirror floats with the output level. With this scheme, Q6 never sees a change in base-collector voltage and does not degrade the gain with its output impedance, which is a factor of 5–10 lower than that of NPNs Q3 and Q4. By choosing I2 so that Q7 runs at twice the collector current of Q5–Q6, the base current of Q7 balances the combined base currents of Q5 and Q6. A benefit of this balanced design is low offset voltage drift (2µV/°C maximum).

The output stage is formed by Q8, Q9, Q10 and Q11 and current sources I5 and I6. This stage further buffers the gain node from the output. The path from the emitter of Q7 to the output has symmetrical current gain, as it contains both an NPN and PNP, whether sourcing or sinking current. This balance reduces 2nd harmonic distortion.

Frequency compensation is set by capacitor C1 on the gain node for a 90MHz gain bandwidth at 100kHz. Capacitor C2 rolls off the mirror gain, which produces a pole-zero pair so that the open-loop response reaches unity gain at 25MHz with 42° of phase margin. C2 is bootstrapped to the output so that it does not degrade slew rate. The gain and phase versus frequency are shown in Figure 4. Slew rate is set by I1 and C1 and is typically 22V/µs.

Design Trade-Offs

Previous precision designs had multiple gain stages and highly balanced configurations. The price paid by these classic designs is lack of

bandwidth, slew rate and settling time. The LT1468 uses a single stage topology to obtain excellent AC specifications with high bandwidth and state-of-the-art 16-bit settling. The demands of precision dictate a fully balanced design and painstaking care in the die layout. The AC performance is ultimately limited, however, by the need for high gain and low input bias current. High gain requires bootstrapping the current mirror in the signal path, which degrades phase margin at high frequency. For this reason the mirror is compensated to lower the unity-gain frequency of the amplifier, which reduces bandwidth at low closed-loop gains.

To obtain low input bias current, the choice of operating currents is limited by the accuracy of the input bias current cancellation circuitry. With trimming, up to a 50× reduction in I_B can be achieved. This constraint sets the maximum value of current source I1, which also places limits on bandwidth, slew rate, noise voltage and noise current. The LT1468 total noise is best with source resistance in the 1kΩ to 20kΩ region, where any increase in noise is due to the resistor (Figure 5).

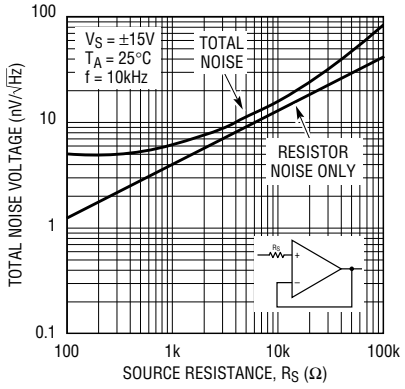

Figure 5. Total noise vs unmatched source resistance

It should be noted that the input bias current cancellation current is not bootstrapped to the input stage to provide constant I_B vs input common mode voltage. The reason is simple: this circuitry runs at submicroamp current levels and has no chance of settling if it is allowed to move with the inputs. The I_B is optimized for inverting configurations with a constant input voltage and provides excellent settling.

Conclusion

The LT1468 has an unequaled blend of speed and precision that is ideal for 16-bit applications. Its unique virtues also provide outstanding performance in low distortion active filters and precision instrumentation.

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LT1676/LT1776, continued from page 9

discrete pulses. The output capacitor must supply the entire load current for at least a portion of the switching cycle, so output capacitor ripple current rating and ESR may be an issue. Maximum available output current will usually be a strong function of input voltage. Supporting low V_{IN}-to-V_{OUT} ratios may require additional components for maintaining control-loop stability. A detailed theoretical analysis of this topology and its behavior can be found in Linear Technology Application Note 44.

Conclusion

The LT1676 and LT1776 provide excellent efficiency in high input voltage/low output voltage switching regulator applications. This LT1776's 8-pin SO package and 200kHz switching rate are especially useful in implementing compact power supply solutions. These devices' innate ability to avoid pulse skipping under light loads, plus the optional sync function, aid in controlling the frequency spectrum of switching-generated noise.

LT1675, continued from page 17

Performance

Table 1 summarizes the major performance specifications of the LT1675; Figure 8 shows a graph of crosstalk.

Conclusion

By taking full advantage of LTC's new complementary high speed bipolar process, the LT1675 RGB multiplexer dramatically raises the level of performance while saving PC board space. A channel-to-channel toggle rate of 100MHz makes the LT1675 perfect for pixel switching and the simple expansion feature using the $\overline{\text{ENABLE}}$ pin is ideal for RGB routing. A fixed gain of two for driving double terminated cables simplifies PC board layout and boosts performance. These high performance multiplexers complement the large number of video products offered by LTC.

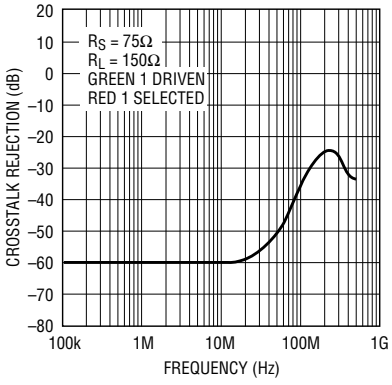


Figure 8. LT1675 crosstalk rejection vs frequency

LTC1622: Low Input Voltage, Current Mode PWM Buck Converter

by San-Hwa Chee

Introduction

The push for 2.5V system supplies continues unabated as manufacturers introduce more parts that operate at this low voltage. The rewards are great, especially for battery-powered equipment, since the lower voltage reduces power consumption and thereby extends the time between battery replacements or recharges. With a 2.5V system supply, operation from a single lithium-ion battery becomes highly attractive, because its end-of-charge voltage is 2.7V and it has the most energy per volume compared to NiCd and NiMH.

The 8-pin LTC1622 step-down DC/DC controller is designed to help system designers harness all of the available energy from lithium-ion batteries in several ways. Its wide operating input-voltage range (2.0V to an absolute maximum of 10V) and 100% duty cycle allows low dropout for maximum energy extraction from the battery. The part's low quiescent current, 400µA, with a shutdown current of 15µA, extends battery life. Its user-selectable Burst Mode operation enhances efficiency at low load current.

For portable applications where board space is a premium, the LTC1622 operates at a constant frequency of 550kHz and can be synchronized to frequencies of up to 750kHz. High frequency operation allows the use of small inductors, making this part ideal for communications products. The LTC1622 comes in a tiny 8-lead MSOP package, providing a complete power solution while occupying only a small area.

The LTC1622 uses a pulse-width, current mode architecture, which provides excellent AC and DC load and line regulation. Peak inductor current is set by an external sense resistor. This allows the design to be optimized for each application. A soft-start pin allows the LTC1622 to power up gently.

A Detailed Look at the LTC1622

The LTC1622 is a constant-frequency, pulse-width-modulated, current mode switching regulator. In normal operation, the external P-channel power MOSFET is turned on during each cycle when the oscillator sets a latch and turned off when the current comparator resets the latch. The peak inductor current at which the current comparator resets the latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier, g_m. An external resistive divider connected between V_{OUT} and ground allows g_m to receive an output feedback voltage, V_{FB}. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which, in turn, causes the I_{TH} voltage to increase until the average inductor current matches the new load current. (For a more detailed description, please refer to the LTC1622 data sheet.)

The value of the R_{SENSE} is chosen based on the required output current. The LTC1622 current comparator has a maximum threshold of 100mV/R_{SENSE}. The current-comparator threshold sets the peak of the inductor current, yielding a maximum average output current equal to the peak value minus one-half the peak-to-peak inductor ripple current. For applications where the duty cycle is

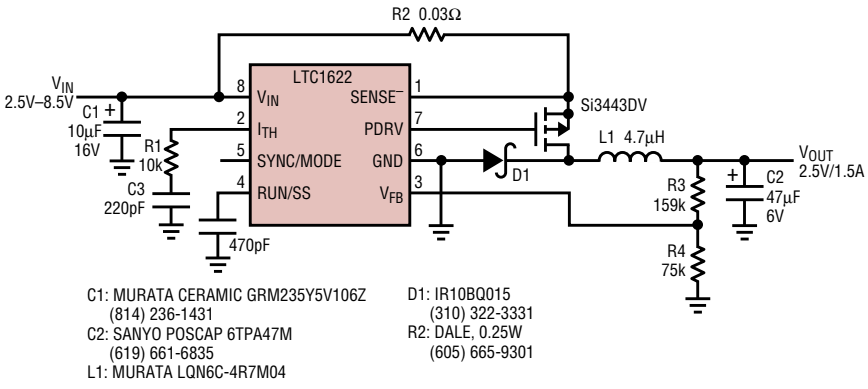


Figure 1. LTC1622 typical application: 2.5V/1.5A converter

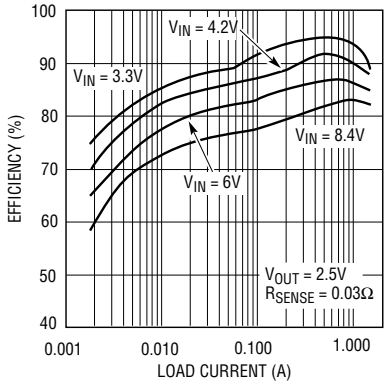


Figure 2. Efficiency vs load current for Figure 1's circuit (Burst Mode enabled)

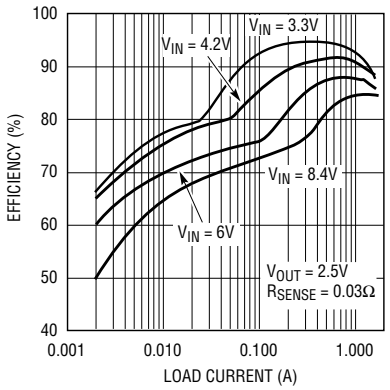


Figure 3. Efficiency vs load current for Figure 1's circuit (Burst Mode disabled)

high (> 80%), the value of the sense resistor is set to approximately 50mV/I_{OUTMAX} to account for the effect of slope compensation. Under short-circuit conditions, the frequency of the oscillator will be reduced to about 120kHz. This low frequency allows the inductor current to safely discharge, thereby preventing current runaway.

The LTC1622 includes protection against output overvoltage conditions or transients. An overvoltage comparator monitors the output voltage and forces the external MOSFET off when the feedback voltage has risen to 8% above the reference voltage (0.8V).

Burst Mode Operation

The LTC1622's Burst Mode operation is enabled at low load currents simply by connecting the SYNC/MODE pin to V_{IN} or letting it float. In this mode, the minimum peak current of the inductor is set to 0.36V/R_{SENSE} even though the voltage at the I_{TH} pin would indicate a lower value. If the inductor's average current is greater than the load requirement, the voltage at the I_{TH} pin will drop as V_{OUT} rises slightly. When the I_{TH} voltage goes below 0.12V, a sleep signal is generated, turning off the external MOSFET. The load current is now supported by the output capacitor. The LTC1622 will resume normal operation when the I_{TH} voltage goes above 0.22V. For frequency-sensitive applications, Burst Mode operation is inhibited by connecting the SYNC/MODE pin to ground. In this case, constant-frequency operation will be maintained at a lower load current together with lower output ripple. If the load current is low enough, cycle skipping will occur to maintain regulation.

Frequency Synchronization

The LTC1622 can be externally driven by a clock signal of up to 750kHz. Synchronization is inhibited when the feedback voltage is below 0.3V. This is done to prevent inductor current build-up under short-circuit conditions. Burst Mode operation is inhibited when the LTC1622 is driven by an external clock.

Undervoltage Lockout and Dropout Operation

An undervoltage lockout circuit is incorporated into the LTC1622. When the input voltage drops below 2.0V, most of the LTC1622 circuitry will be turned off, reducing the quiescent current from 400µA to several microamperes and forcing the external MOSFET off.

The LTC1622 is capable of turning the external P-channel MOSFET on continuously (100% duty cycle) when the input voltage falls to near the output voltage. In dropout, the output voltage is determined by the input voltage minus the voltage drop across the MOSFET, the sense resistor and the inductor resistance.

RUN/Soft-Start Pin

The RUN/SS pin is a dual-function pin that provides the soft-start function and a means to shut down the LTC1622. An internal current source charges an external capacitor. When the voltage on the Run/SS pin reaches 0.65V, the LTC1622 begins operating. As the voltage on the RUN/SS continues to increase linearly from 0.65V to 1.8V, the internal current limit also increases proportionally. The current limit begins at 0A (at $V_{RUN/SS}$ = 0.65V) and ends at 0.10V/R_{SENSE} ($V_{RUN/SS}$ > 1.8V); therefore, this pin can be used for power supply sequencing.

2.5V/1.5A Step-Down Regulator

A typical application circuit using the LTC1622 is shown in Figure 1. This circuit supplies a 1.5A load at 2.5V with an input supply between 2.7V up to 8.5V. The 0.03Ω sense resistor is selected to ensure that the circuit is capable of supplying 1.5A at a low input voltage. In addition, a sublogic threshold MOSFET is used, since the circuit operates at input voltages as low as 2.7V. The circuit operates at the internally set frequency of 550kHz. A 4.7µH inductor is chosen so that the inductor's current remains continuous during burst periods at low load current. For low output voltage ripple, a low ESR capacitor (100mΩ) is used.

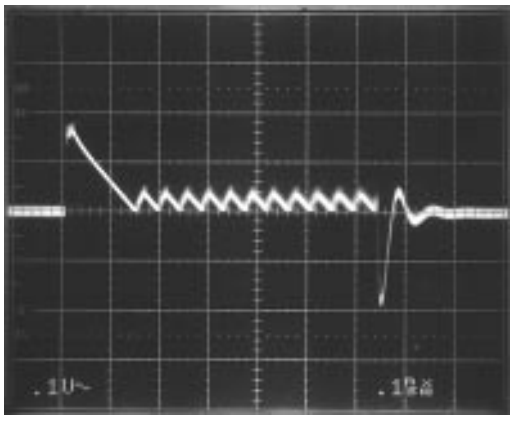


Figure 4. Transient response with Burst Mode enabled; load step = 50mA to 1.2A

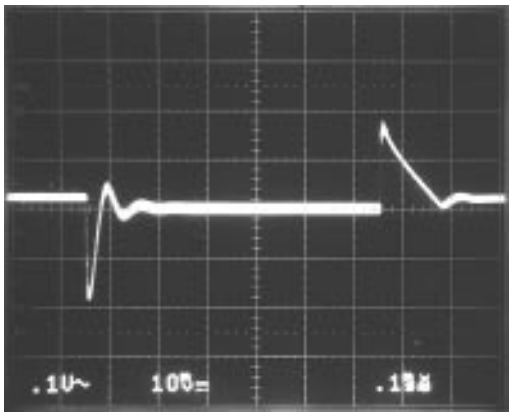


Figure 5. Transient response with Burst Mode inhibited; load step = 50mA to 1.2A

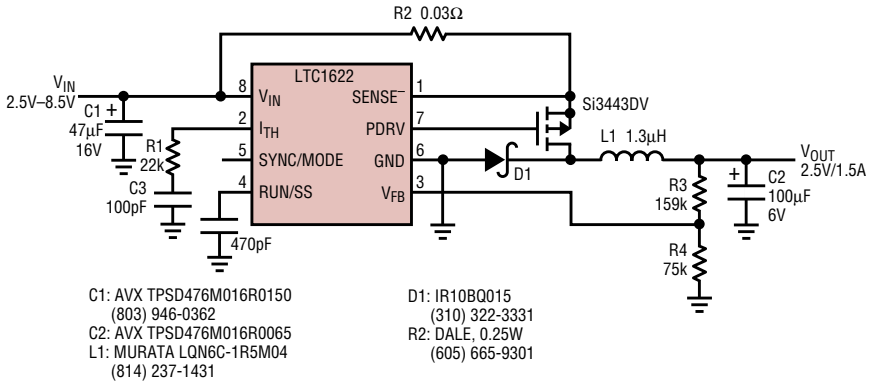


Figure 6. 2.5V/1.5A converter with improved transient response

Efficiency Considerations

The efficiency curves for Figure 1's circuit are shown in Figures 2 and 3. Figure 2 shows the efficiency with Burst Mode enabled, whereas Figure 3 has Burst Mode defeated. Note that, at low load currents, the efficiency is higher with Burst Mode operation. However, constant frequency operation is still achievable at a lower load currents with Burst Mode operation defeated. The kinks in the efficiency curves indicate the transition out of Burst Mode operation.

The components of Figure 1 have been carefully chosen to provide the amount of output power using a minimum of board space. Efficiency is also a prime consideration in selecting the components, as illustrated in Figures 2 and 3. Figures 4 and 5 show the transient response of V_{OUT} with a load step from 50mA to 1.2A. Figure 4 has Burst Mode enabled, while Figure 5 has it defeated. Note that the output voltage ripple (in the middle portion of the photographs) is higher for Burst Mode operation than with Burst Mode disabled at 50mA load current.

Applications that require better transient response can use the circuit in Figure 6, whose components are selected specifically for this requirement. Figures 7 and 8 show the response with and without Burst Mode operation, respectively. Note that the transient response has been enhanced significantly. However, this comes at the expense of slightly reduced efficiency at low load currents, as indicated by the efficiency curves of Figures 9 and 10.

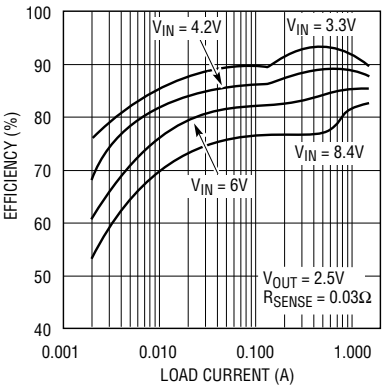


Figure 9. Efficiency vs load current for Figure 6's circuit (Burst Mode enabled)

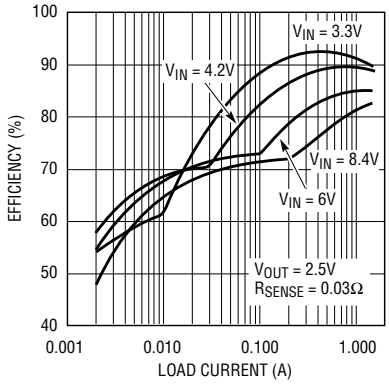


Figure 10. Efficiency vs load current for Figure 6's circuit (Burst Mode disabled)

Conclusion

Although the LTC1622 comes in a tiny 8-pin MSOP, it is packed with features that are not normally found in other DC/DC converters. Its ability to operate from input voltages as low as 2.0V makes it attractive for single lithium-ion battery-powered applications. Features like Burst Mode and 100% duty cycle ensure that energy from the battery is used efficiently and charge is extracted down to the last coulomb. For telecommunications products, where noise generated by a switching regulator may spell trouble, the synchronizable LTC1622 can operate at a constant frequency, making noise a nonissue for system designers.

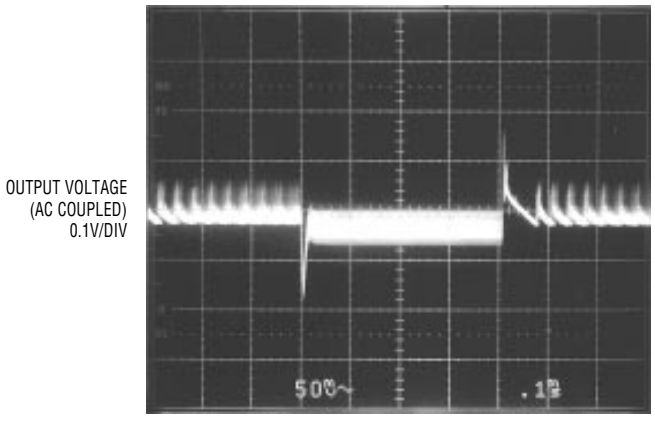


Figure 7. Transient response with Burst Mode enabled; load step = 50mA to 1.2A

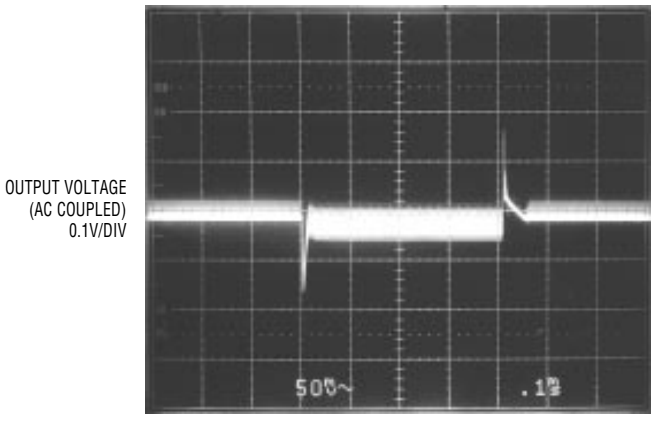


Figure 8. Transient response with Burst Mode inhibited; load step = 50mA to 1.2A

LTC1531 Isolated Comparator

by Wayne Shumaker

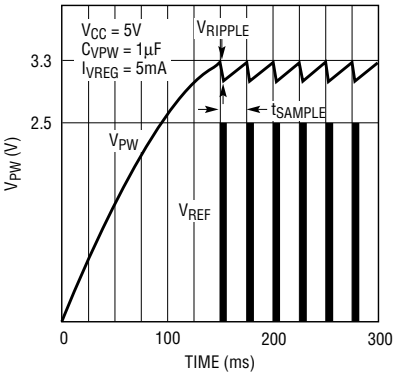
Introduction

The LTC1531 is an isolated, self-powered comparator that receives power and communicates through internal isolation capacitors. The internal isolation capacitors provide $3000V_{RMS}$ of isolation between the comparator and its output. This allows the part to be used in applications that require high voltage isolated sensing without the need to provide an isolated power source. The isolated side provides a 2.5V pulsed reference output that can deliver 5mA for 100µs using the power stored on the isolated external capacitor. A 4-input, dual-differential comparator samples at the end of the reference pulse and transmits the result back to the nonisolated side. The nonisolated, powered side latches the result of the comparator and provides a zero-cross comparator output for triggering a triac. Typical applications include isolated temperature sensing and control, isolated voltage monitoring and other sensing applications riding on top of high common mode voltages, such as the AC power line.

Basic Operation

The block diagram in Figure 1 shows the basic components of the LTC1531. The nonisolated powered side toggles between pumping AC voltage through the capacitive barrier to the isolated side, where it is rectified and stored on an external capacitor tied to V_{PW}, and listening for a comparison result. When the isolated-side V_{PW} voltage reaches 3.3V, the comparison circuitry is enabled. On the next listen cycle, the 2.5V V_{REG} output pulses on for 100µs, at the end of which a comparison is done, with the result transmitted back to the nonisolated side. If a valid result is received, the DATA output is updated and the VALID output pulses on for 1ms. When the latched DATA output is high, the zero-cross comparator output is enabled for firing a triac whenever the zero-cross comparator inputs pass through 0V.

Figure 2 represents a typical V_{PW} start-up sequence, showing V_{REG} output pulses after V_{PW} reaches 3.3V. Thereafter, whenever V_{PW} reaches 3.3V the comparator samples during the next listen period in the power/listen cycle. Figure 2 shows typical sampling with light loading on V_{REG}. Sampling is not uniform but depends on the combination of V_{PW} = 3.3V and the 800Hz power/listen cycle. The comparator samples at a typical rate of 200Hz–300Hz. The actual sampling rate depends on the internal and external loading on the 2.5V V_{REG} output and the charging rate to the



NOTES: V_{RIPPLE} DEPENDS ON C_{VPW} AND $I_{VPW} + I_{VREG}$
t_{SAMPLE} DEPENDS ON $I_{VPW} + I_{VREG}$

Figure 2. Typical V_{PW} power-up and V_{REG} samples

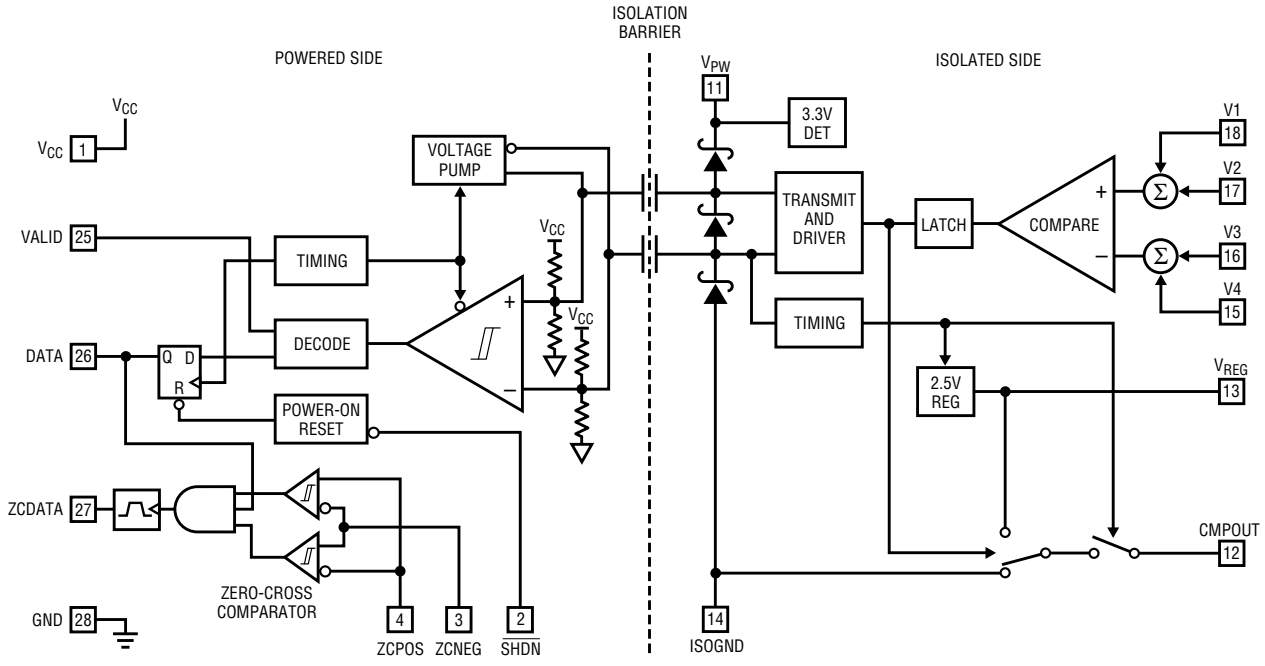
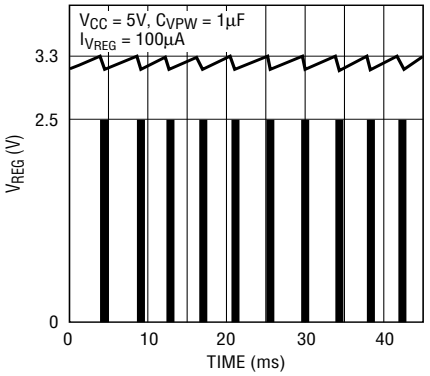


Figure 1. LTC1531 block diagram



NOTE: NONPERIODIC SAMPLES DUE TO DEPENDENCE ON V_{PW} > 3.3V AND THE POWER-LISTEN CYCLE SAMPLING

Figure 3. Typical V_{REG} and V_{PW} with $I_{V_{REG}}$ = 100µA

external capacitor on V_{PW}. This charging rate, through the internal isolation capacitors to V_{PW}, can be modeled as a 100k source resistance and a 5.5V source with V_{CC} = 5V. Figure 4 shows typical sampling periods for different load currents and supply voltages. The sample rate does not depend on the external storage capacitor, whose value should be chosen to minimize ripple on V_{PW} for different V_{REG} loads. V_{PW} can also be used to power continuous, low current circuits, such as the LT1495 op amp or the LTC1540 comparator, provided that such circuits do not prevent V_{PW} from reaching 3.3V.

Isolated Comparator

The LTC1531 isolated switched capacitor comparator has four inputs that sum the voltages together to perform the following comparison:

(V1 + V2)/2 > (V3 + V4)/2

By rearranging the equation, for example, a dual differential comparison can be performed:
(V1 – V4) > (V3 – V2) or (V1 – V3) > (V4 – V2)

The comparator inputs have a rail-to-rail input range. They sample once at the end of the 100µs V_{REG} pulse. Their summing nature allows mid-V_{REG} referencing, for example, by connecting V3 to V_{REG} and V4 to ISOGND, which sums together to provide 1.25V for the negative comparator input. In the isolated temperature control application (Figure 5), the comparator is used to compare the voltage across the thermistor to the voltage across R4, with (V1 – V3) > (V4 – V2).

The isolated comparator has an isolated output, CMPOUT, which can be used for hysteresis. This output is Hi-Z except when V_{REG} is on; then the output is either 2.5V or 0V, depending on the result of the previous comparison. This output, in combination with the comparator, can be used to create a delta-sigma modulator for transmitting isolated voltage signals across the isolation barrier, as in the isolated voltage sense application (Figure 6).

Applications

The LTC1531 can be used to isolate sensors such as in the isolated thermistor temperature controller in Figure 5. In this circuit, a comparison is made between the voltages across a

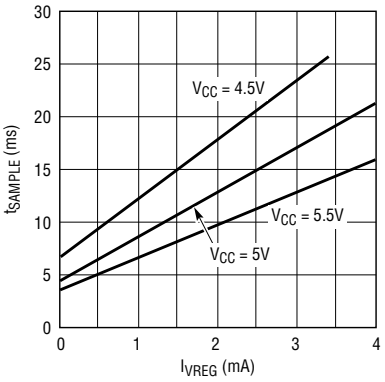


Figure 4. Typical average t_{SAMPLE} vs $I_{V_{REG}}$

thermistor and a resistor that is driven by the 2.5V V_{REG} output. As the thermistor resistance rises with temperature, the voltage across the thermistor increases. When it exceeds the voltage across R4, the comparator output becomes zero and the triac control to the heater is turned off. Hysteresis can be added in the temperature control by using CMPOUT and R5. A 10° phase-shifted AC line signal is supplied through R1, R2 and C1 to the zero-cross comparator for firing the triac.

In the overtemperature detect application in Figure 6, an isolated thermocouple is cold junction compensated with the micropower LT1389 reference and the Yellow Springs thermistor. The micropower LT1495 op amp provides gain to give an overall 0°C–200°C temperature range, adjustable by changing the 10M feedback resistor. The isolated comparator is connected to compare at 1.25V or

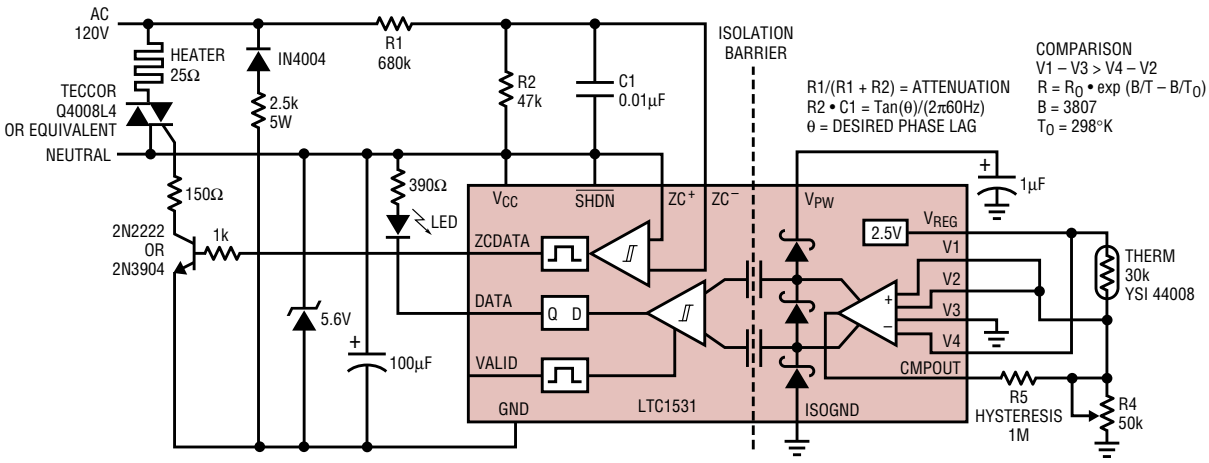


Figure 5. Isolated thermistor temperature controller

the center of the temperature range. In this case, V_{TRIP} goes high when the temperature exceeds 100°C.

The LTC1531 can use the high impedance nature of CMPOUT as a duty-cycle modulator, as in the isolated voltage sense application in Figure 7. The duty-cycle output of the comparator is smoothed with the LT1490 rail-to-rail op amp to reproduce the voltage at V_{IN}. The output time constant, R2 • C2, should approximately equal the input time constant, 35 • R1 • C1. The factor of 35 results from CMPOUT being on for only 100µs at an average sample rate of 300Hz.

Conclusion

The LTC1531 is a versatile part for sensing signals that require large isolation voltages. The ability of the LTC1531 to supply power through the isolation barrier simplifies applications; it can be combined with other micropower circuits in a variety of isolated signal conditioning and sensing applications.

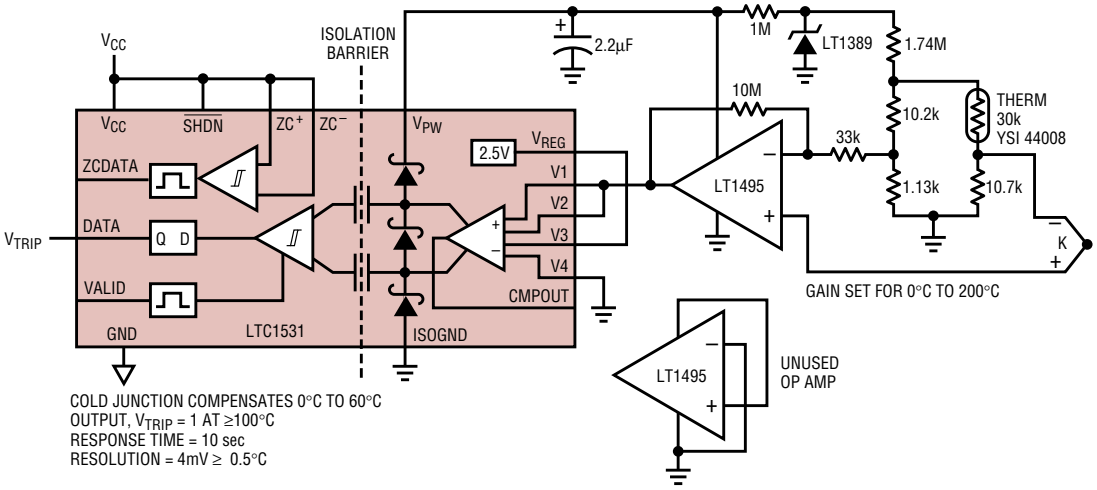


Figure 6. Overtemperature detect

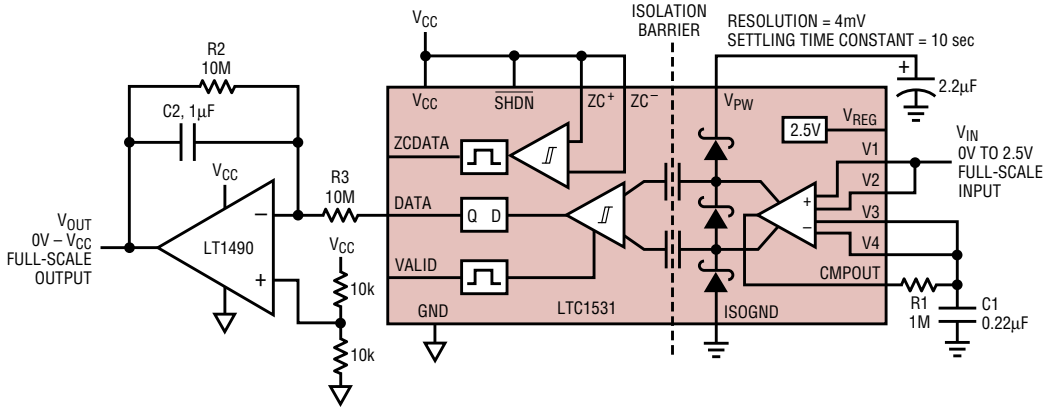


Figure 7. Isolated voltage detect

PolyPhase Switching Regulators Offer High Efficiency in Low Voltage, High Current Applications

by Craig Varga

Introduction

In recent years, there has been a tendency in the digital world toward smaller device geometries and higher gate counts. This has led to requirements for lower voltages and higher currents for logic supplies. As this trend continues, to levels under 2V and over 30A, the conventional buck regulator approach ceases to be viable. Switch currents are too high for a single device to handle, inductor energy storage exceeds what is available in surface mount technology and ripple current requirements on input capacitors dictate the use of many capacitors in parallel. Although all this may seem like enough of a challenge, the transient response requirements also become much more severe. The question that arises is: "is there a topology that can solve all of these problems simultaneously?" The answer is "PolyPhase™."

What is PolyPhase, Anyway?

Since it is apparent that multiple FETs need to be paralleled to handle the current requirements, the question is whether there is a way to drive them intelligently, rather than by brute force. The solution is to stagger the turn-on times so that the dead bands in the input current waveform are "filled up," so to speak. In the simplest implementation, there are essentially two independent synchronous buck regulators operating 180°

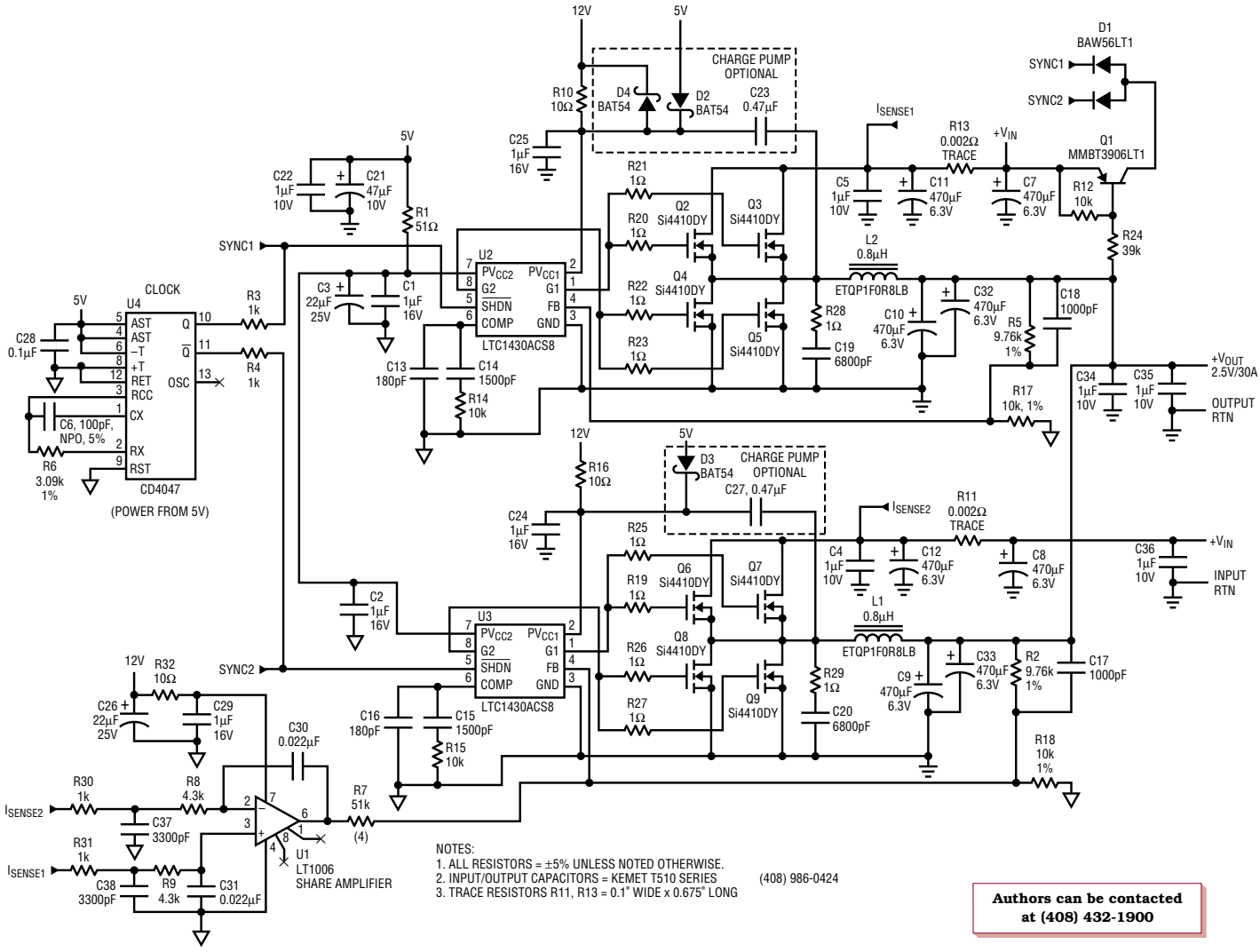
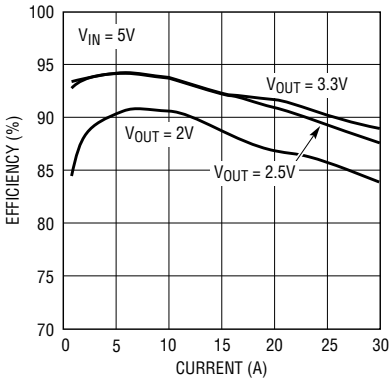


Figure 1. 2-phase synchronous buck regulator



Efficiency of Figure 1's circuit, V_{IN} = 5V

out of phase. The net effect of this is that the input and output ripple currents of the two channels tend to cancel during steady-state operation. This results in significant reductions in both input and output capacitor requirements. There is also a fourfold reduction in the total inductor energy storage requirement, which means much smaller inductors and vastly improved transient dynamics. During a large load step, the two channels operate at maximum duty factor in an attempt to maintain the desired output voltage. Both inductor currents slew rapidly and are now additive, since they are going in the same direction. Hence, the slew rate is double what a single channel could do for equal inductor values. However, due to the ripple current cancellation during steady-state conditions, the two inductors can be reduced to approximately one-half the value that a single channel design would require for equal ripple currents. Since during slew they appear to be operating in parallel, the actual slew rate is four times that of a single channel design with equal steady-state output ripple current. Both input and output ripple frequencies are double those of a single-channel design, further simplifying filtering requirements.

Why Stop at Two?

If two channels are good, aren't more channels better? In a word, yes. In principle, there is no limit to the number of parallel channels that can be added. As the number of channels, *n*, increases, the ripple frequency increases to *n* times the single-channel frequency. Input and output RMS ripple currents continue to decrease. Diminishing returns are reached as *n* rises above three. At three stages, the ripple reductions are very substantial and dynamic performance is excellent. Adding more channels produces slight improvements but the dramatic gains will have been realized by *n* = 3. The only real penalty is added complexity.

Another aspect worth considering is expandability. It is reasonable with today's technology to build a single stage, all surface mount, synchronous buck regulator capable of approximately 15 amps continuous output current. At higher current levels, power dissipation in individual devices becomes difficult to manage. Gate drive capability of driver ICs is somewhat limited and is incapable of driving enough paralleled MOSFETs to handle larger currents at high frequencies. Inductors capable of greater energy storage cannot be obtained in surface mount technology. Therefore, if currents substantially greater than 15 amps are required, it is a simple matter of paralleling additional stages to obtain the higher currents. For 30 amps, use two stages. At 45 amps, use three stages and so on. As more stages are added, the ripple currents are further reduced, so there is no need to add large quantities of input or output capacitors to handle the higher current capability.

The bottom line is that PolyPhase designs offer a considerable reduction in the cost and volume of the power devices at the expense of a little added complexity in the control circuitry.

2-Phase Design Example

The circuit shown in Figure 1 is a 2-phase, voltage mode–control, synchronous buck regulator designed for a 5V input and output voltages below 3.3V. It is intended to power large memory arrays, ASICs, FPGAs and the like in server and workstation applications. The output is capable of more than 30 amps continuous at outputs of 2.5V and below, with peak current capability of greater than 40 amps. The design is entirely surface mount and the maximum height above the board is 5.5mm. Overall board area is only 4.24 in^2. Efficiency is excellent, as can be seen in the curve in Figure 2. Output ripple voltage is shown in Figure 3. The circuit's dynamic response to a 10 amp load step is shown in Figure 4. The

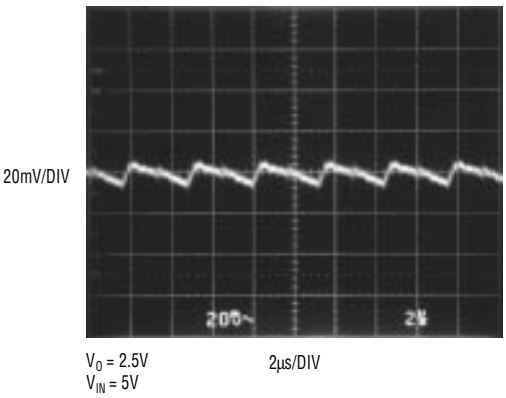


Figure 3. Output ripple with 30A load

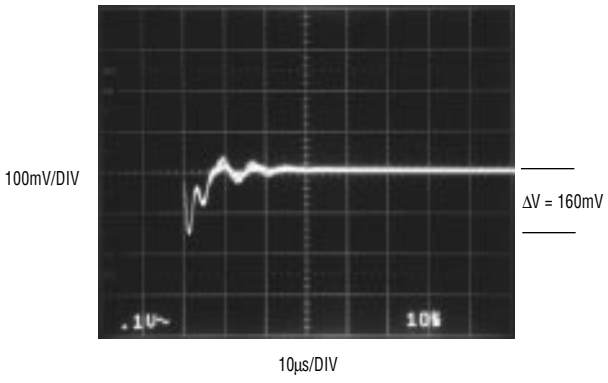


Figure 4. Transient response with 10A load step (100ns rise time)

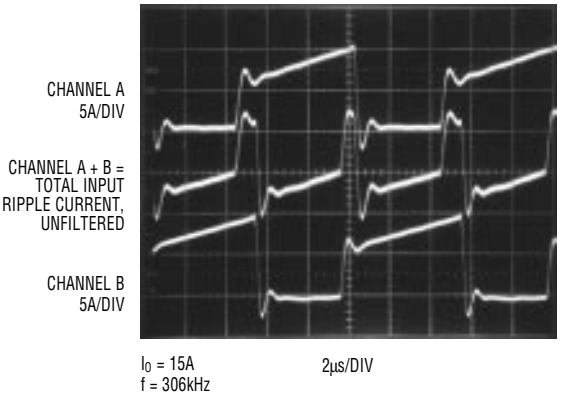


Figure 5. Ripple cancellation—input

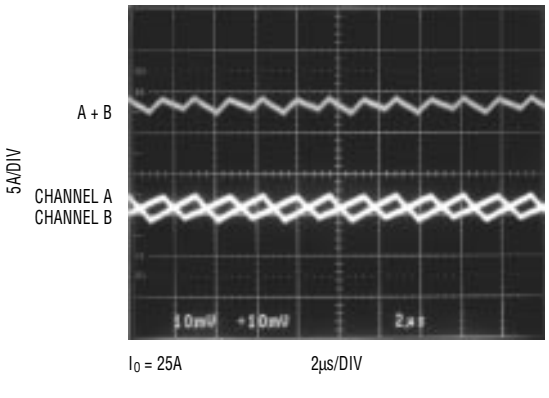


Figure 6. Ripple cancellation—output

response is dominated by the output capacitor's ESR and shows the output voltage recovered to the original level in under 10µs. Figures 5 and 6 show how the input and output ripple currents cancel.

Circuit Operation

The basic design consists of two LTC1430CS8-based synchronous buck regulators connected in parallel and operated 180° out of phase. U4, the CD4047 oscillator, is used to generate the required clock signals and synchronize the two LTC1430s. Unfortunately, simply connecting two regulators in parallel is a recipe for instant disaster. The output voltages of the two regulators will be slightly different due to normal component tolerances. Therefore, the higher output voltage channel will attempt to supply the full load current, while the lower voltage output will sink current from the output in a desperate attempt to reduce the output voltage to where it thinks it should be. The result is like a dog chasing its tail, with large currents running around in a circle and going nowhere.

Op amp U1 solves this problem. Because the two channels are identical, if the output currents are the same, the input currents will be also. Low value sense resistors are included in the input power path to allow the circuit to measure input current. U1 then forces the input current of channel two to match the input current of channel one by making small adjustments in channel two's output voltage. It does this by adding or subtracting a small amount of current from channel two's feedback divider. The two sense resistors are short lengths of PCB trace and only need to be ratiometrically accurate. Absolute value of these resistors is not important (see Linear Technology Application Note 69, Appendix A, for a discussion on how to design trace resistors).

The only remaining trick in the circuit is the role of Q1 and its associated circuitry. At start-up, the LTC1430's clock frequency is slowed down to approximately 10kHz until the output voltage rises to approximately 50% of the desired level. If, during this start-up phase, an attempt is made to synchronize the controller to a very high frequency, the oscillator ramp amplitude never rises to a level sufficiently high to trip the PWM comparator and enable the FET drivers. Therefore, the output gets stuck on ground. Q1 fixes this by forcing the sync signals high during the turn-on transient. Once the output voltage nears its final level, the clock signals are allowed to synchronize the two PWM controllers.

Conclusion

The design shown combines the performance characteristics that will be required to power the digital systems that will emerge over the next several years. Circuits based on these concepts will be able to efficiently deliver very high current at low voltage while relying on surface mount technology to maintain low profile and minimum use of real estate. They will also provide substantially better dynamic performance than has been available using more conventional design methodologies and do all of this at a reasonable cost.

Level Shift Allows CFA Video Amplifier to Swing to Ground on a Single Supply

by Frank Cox

A current feedback (CFA) video amplifier can be made to run off a single supply and still amplify ground-referenced video with the addition of a simple and inexpensive level shifter. The circuit in Figure 1 is an amplifier and cable driver for a current output video DAC. The video can be composite or component but it must have sync. The single positive supply is 12V but could be as low as 6V for the LT1227.

The output of the LT1227 CFA used here can swing to within 2.5V of the negative supply with a 150Ω load over the commercial temperature range of 0°C to 70°C. Five diodes in the feedback loop are used, in conjunction with C5, to level shift the output to ground. The video from the output of the LT1227 charges C5 and the voltage across it allows the output to swing to ground or even slightly negative. However, the level of this negative swing will depend on the video signal and so will be unpredictable. When the scene is black, there must be sync on the video for C5 to remain charged. A zero-level component video signal with no sync will not work with this circuit. The CFA output will try to go to zero, or as low as it can, and the diodes will turn off. The load will be disconnected from the CFA output and connected through the feedback resistor to the network of R6 and R7. This causes about 150mVDC to appear at the output, instead of the 0V that should be there.

The ground-referenced video signal at the input needs to be level shifted into the input common mode range of the LT1227 (3V above negative supply). R4 and R5 shift the input signal to 3V. In the process, the input video is attenuated by a factor of 2.5. For correct gain, no offset and with a zero source impedance, R4 would be 1.5k. To compensate for the presence of R3, R4 is made 1.5k minus R3, or 1.46k. The trade off is a gain error of about 1.5%. If R4 is left 1.5k, the gain is correct, but there is an offset error of 75mV. R6, R7 and R8 set the gain and the output offset of the amplifier. A noninverting gain of five is taken to compensate for the attenuation in the input level shifter and the cable termination.

The voltage offset on the output of this circuit is a rather sensitive function of the value of the input resistors. For instance, an error of 1% in the value of R6 will cause an offset of 30mV (1% of 3V) on the output. This is in addition to the offset error introduced by the op amp. Precision resistor networks are available (BI technologies, 714-447-2345) with matching specifications of 0.1% or better. These could be used for the level shifting resistors, although this would make adjustments like the one made to R4 difficult.

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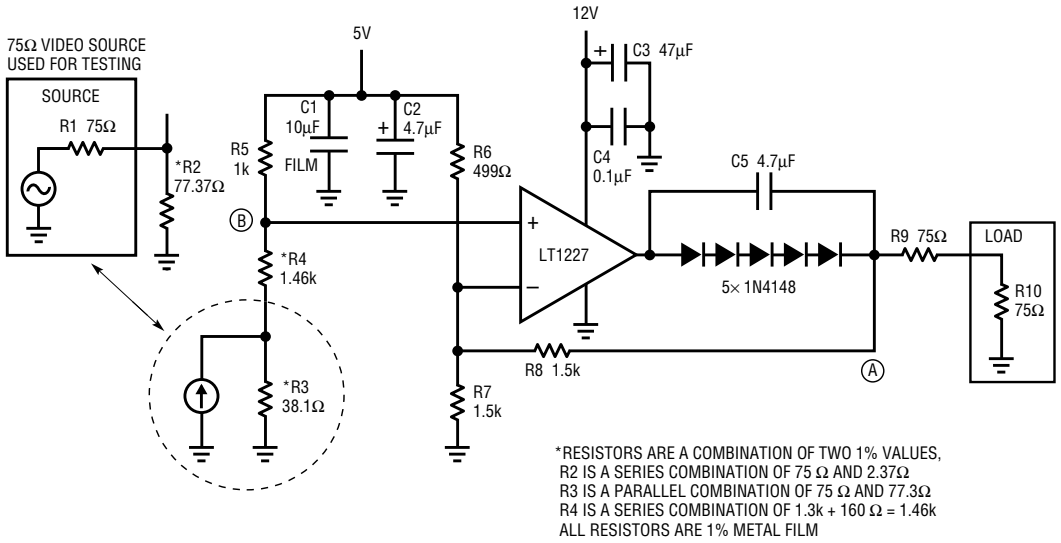

Figure 1. Amplifier and cable driver for current-output video DAC

Component and Measurement Advances Ensure 16-Bit DAC Settling Time (Part Two)

by Jim Williams

Introduction

Reliable measurement of 16-bit DAC settling time is extremely challenging. Part one of this article (in the August 1998 issue of *Linear Technology* magazine) described a method for making this measurement. This second part discusses detailed circuitry and presents results.

Detailed Settling-Time Circuitry

Figure 1 is a detailed schematic of the 16-bit DAC settling-time-measurement circuitry. The input pulse switches all DAC bits simultaneously and is also routed to the oscilloscope via a delay-compensation network. The delay network, composed of CMOS inverters and an adjustable RC network, compensates the oscilloscope's input step signal for the 12ns delay through the circuit's measurement path. The DAC amplifier's output is compared against the LT1236-10V reference via the precision 3k summing resistor ratio set. The LT1236 also furnishes the DAC reference, making the measurement ratiometric. The clamped settle node is unloaded by A1, which drives the sampling bridge. Note the additional clamp diodes at A1's output. These diodes prevent any possibility of abnormal A1 outputs (due to lost supply or supply sequencing anomalies) from damaging the diode array. A3 and associated components tem-

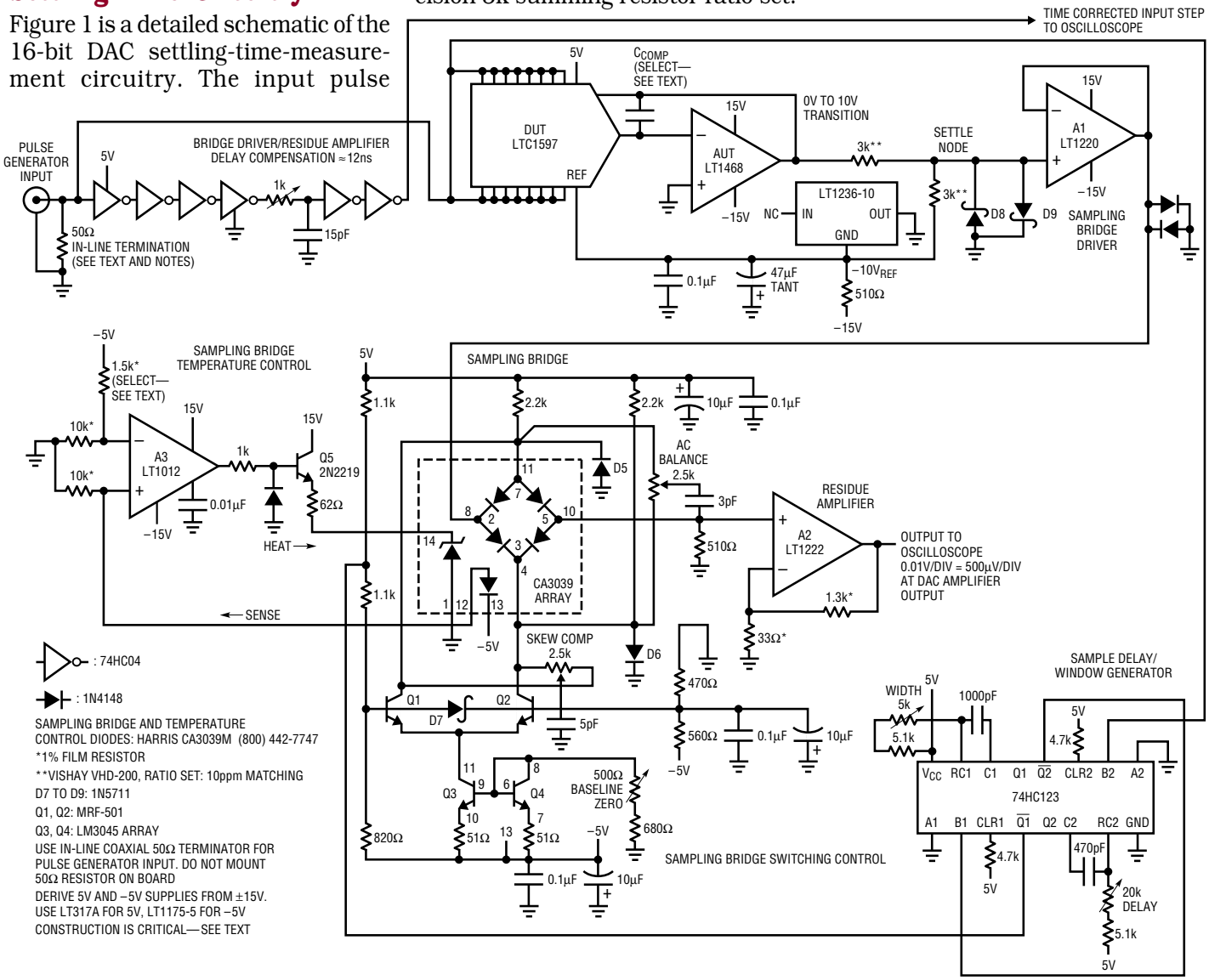

Figure 1. Detailed schematic of DAC-settling-time measurement circuit; optimum performance requires attention to layout.

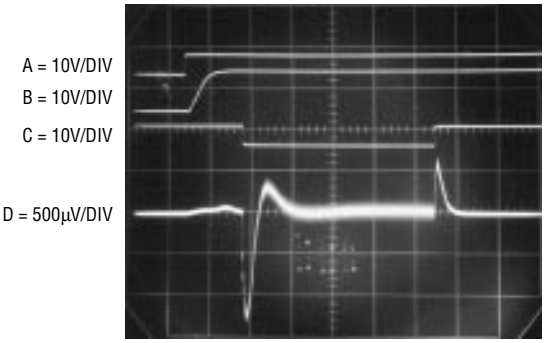

Figure 2. Settling time circuit waveforms include time-corrected input pulse (Trace A), DAC amplifier output (Trace B), sample gate (Trace C) and settling-time output (Trace D). The sample gate window's delay and width are variable.

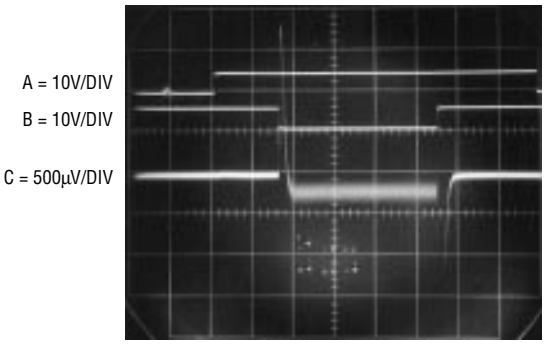

Figure 3. Settling time circuit's output (Trace C) with unadjusted sampling bridge AC and DC trims. The DAC is disabled and the settle node grounded for this test. Excessive switch-drive feedthrough and baseline offset are present. Traces A and B are the input pulse and sample window, respectively.

perature control the sampling diode bridge by comparing a diodes's forward drop to a stable potential derived from the –5V regulator. Another diode, operated in the reverse direction ($V_Z \approx$ 7V) serves as a chip heater. The pin connections shown on the schematic have been selected to provide the best temperature-control performance.

The input pulse triggers the 74HC123 one shot. The one shot is arranged to produce a delayed (controllable by the 20k potentiometer) pulse whose width (controllable by the 5k potentiometer) sets diode bridge on-time. If the delay is set appropriately, the oscilloscope will not see any input until settling is nearly complete, eliminating overdrive. The sample window width is adjusted so that all remaining settling activity is observable. In this way, the oscilloscope's output is reliable and meaningful data may be taken. The one shot's output is level shifted by the Q1–Q4 transistors, providing complementary switching drive to the bridge. The actual switching transistors, Q1–Q2, are UHF types, permitting true differential bridge switching with less than 1ns of time skew.

A2 monitors the bridge output, provides gain and drives the oscilloscope. Figure 2 shows circuit waveforms. Trace A is the input pulse, trace B the DAC amplifier output, trace C the sample gate and trace D the residue amplifier output. When the sample gate goes low, the bridge switches cleanly and the last 1.5mV of slew are easily observed. Ring time is also clearly visible and the amplifier settles nicely to final value. When the sample gate goes high, the bridge switches off, with only 600µV of feedthrough. The 100µV peak before bridge switching (at ≈3.5 vertical divisions) is feedthrough from A1's output, but it is similarly well controlled. Note that there is no off-screen activity at any time—the oscilloscope is never subjected to overdrive.

The circuit requires trimming to achieve this level of performance. The bridge temperature control point is set by grounding Q5's base prior to applying power. Next, apply power and measure A3's positive input with respect to the –5V rail. Select the indicated resistor (1.5k nominal) for a voltage at A3's negative input (again, with respect to –5V) that is 57mV below the positive input's value. Unground Q5's base and the circuit will control the sampling bridge to about 55°C:

$$25°C\ ROOM + \frac{57mV}{1.9mV/°C\ DIODE\ DROP} = 30°C\ RISE = 55°C$$

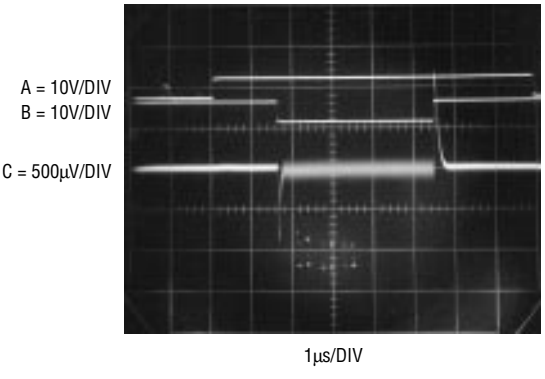

Figure 4. The settling time circuit's output (Trace C) with the sampling bridge trimmed. As in Figure 3, the DAC is disabled and the settle node grounded for this test. Switch drive feedthrough and baseline offset are minimized. Traces A and B are the input pulse and sampling gate, respectively.

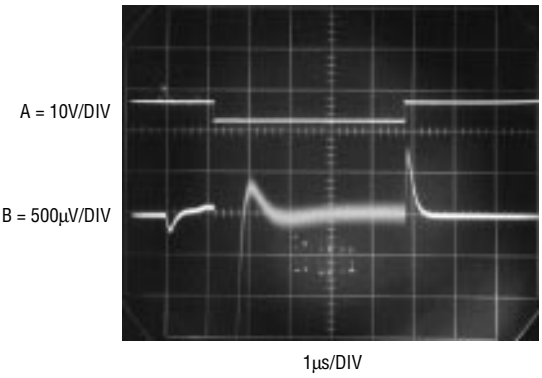

Figure 5. Oscilloscope display with inadequate sample gate delay: the sample window (Trace A) occurs too early, resulting in off-screen activity in the settle output (Trace B). The oscilloscope is overdriven, making displayed information questionable.

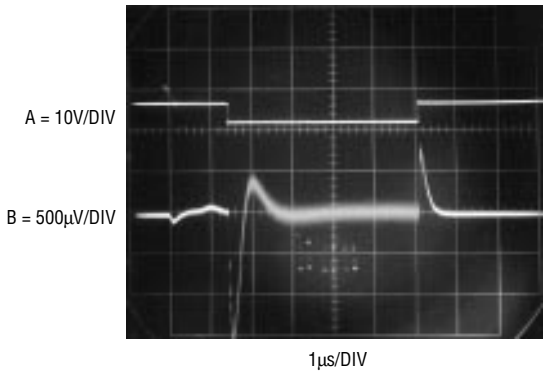

Figure 6. Increasing the sample-gate delay positions the sample window (Trace A) so settle output (Trace B) activity is on-screen.

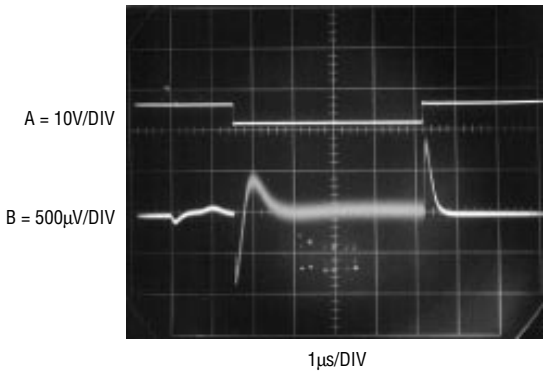

Figure 7. Optimal sample-gate delay positions the sampling window (Trace A) so that all settle output (Trace B) information is well inside screen boundaries.

The DC and AC bridge trims are made once the temperature control is functional. Making these adjustments requires disabling the DAC and amplifier (disconnect the input pulse from the DAC and set all DAC inputs low) and shorting the settle node directly to the ground plane. Figure 3 shows typical results before trimming. Trace A is the input pulse, trace B the sample gate and trace C the residue amplifier output. With the DAC-amplifier disabled and the settle node grounded, the residue amplifier output should (theoretically) always be zero. The photo shows this is not the case for an untrimmed bridge. AC and DC errors are present. The sample gate's transitions cause large, off-screen residue amplifier swings (note residue amplifier's response to the sample gate's turn-off at the ≈8.5 vertical division). Additionally, the residue amplifier output shows significant DC offset error during the sampling interval. Adjusting the AC balance and skew compensation minimizes the switching induced transients. The DC offset is adjusted out with the baseline zero trim. Figure 4 shows the results after making these adjustments. All switching-related activity is now well on-screen and offset error is reduced to unreadable levels. Once this level of performance has been achieved, the circuit is ready for use. Unground the settle node and restore the input pulse connection to the DAC.

Using the Sampling-Based Settling Time Circuit

Figures 5 through 7 underscore the importance of positioning the sampling window properly in time. In Figure 5 the sample gate delay initiates the sample window (trace A) too early and the residue amplifier's output (trace B) overdrives the oscilloscope when sampling commences. Figure 6 is better, with only slight off-screen activity. Figure 7 is optimal. All amplifier residue is well inside the screen boundaries.

In general, it is good practice to "walk" the sampling window up to the last millivolt or so of amplifier slewing so that the onset of ring time is observable. The sampling based approach provides this capability and it is a very powerful measurement tool. Additionally, remember that slower amplifiers may require extended delay and/or sampling window times. This may necessitate larger capacitor values in the 74HC123 one-shot timing networks.

Compensation Capacitor Effects

The DAC amplifier requires frequency compensation to get the best possible settling time. The DAC has appreciable output capacitance, complicating amplifier response and making careful compensation capacitor selection even more important. Figure 8 shows effects of very light compensation.

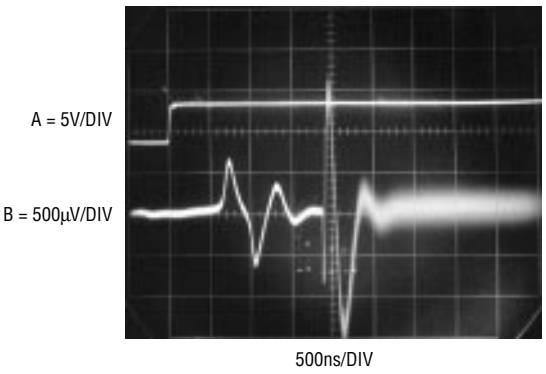

Figure 8. This settling profile with inadequate feedback capacitance shows underdamped response. Excessive ringing feeds through during the sample gate off-period (third through ≈ sixth vertical divisions) but is tolerable (t_{SETTLE} = 2.8μs).

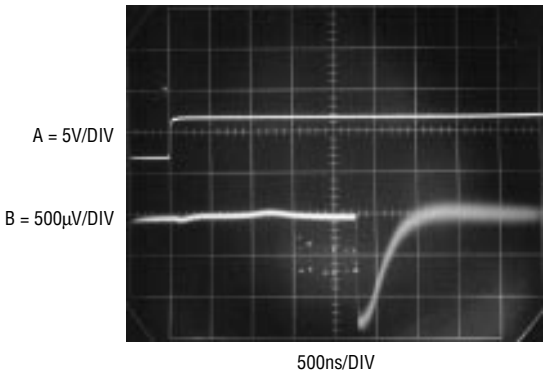

Figure 9. Excessive feedback capacitance overdamps response (t_{SETTLE} = 3.3μs).

Trace A is the time-corrected input pulse and trace B the residue amplifier output. The light compensation permits very fast slewing but excessive ringing amplitude over a protracted time results. The ringing is so severe that it feeds through during a portion of the sample gate off-period, although no overdrive results. When sampling is initiated (just prior to the sixth vertical division) the ringing is seen to be in its final stages, although still offensive. Total settling time is about 2.8µs. Figure 9 presents the opposite extreme. Here, a large value compensation capacitor eliminates all ringing but slows down the amplifier so much that settling stretches out to 3.3µs. The best case appears in Figure 10. This photo was taken with the compensation capacitor carefully chosen for the best possible settling time. Damping is tightly controlled and settling time goes down to 1.7µs.

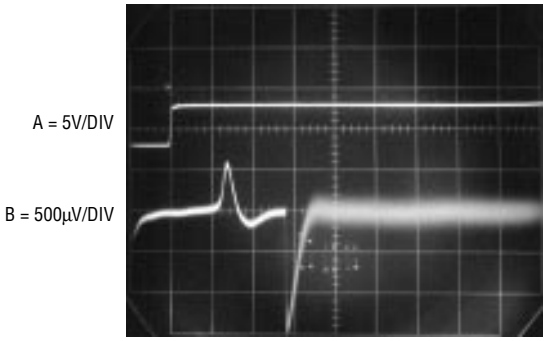

Figure 10. Optimal feedback capacitance yields a tightly damped signature and the best settling time (t_{SETTLE} = 1.7µs).

Settling Times of Various Amplifiers

The previous results, using the LT1468 amplifier, provide extremely fast settling times with high accuracy over temperature. Many applications can tolerate reduced speed, reduced temperature stability or both. Settling times for a number of amplifiers, along with commentary, can be found in LTC Application Note 74, Figure 34. "Optimized" settling times were recorded after individually trimming the feedback capacitors. The "conservative" times represent the worst-case settling times using standard-value compensation capacitors with no trimming.

Conclusion

The sampling-based settling-time circuit appears to be a very useful measurement solution. Expanded discussion and tutorial appear in this article's "root" publication: LTC *Application Note 74, Component and Measurement Advances Ensure 16-Bit DAC Settling Time.*

Net1 and Net2 Serial Interface Chip Set Supports Test Mode

by David Soo

Some serial networks use a test mode to exercise all of the circuits in the interface. The network is divided into local and remote data terminal equipment (DTE) and data-circuit-terminating equipment (DCE), as shown in Figure 1. Once the network is placed in a test mode, the local DTE will transmit on the driver circuits and expect to receive the same signals back from either a local or remote DCE. These tests are called local or remote loopback.

As introduced in the February 1998 issue of *Linear Technology*, the LTC1543/LTC1544/LTC1344A chip set has taken the integrated approach to multiple protocol. By using this chip set, the Net1 and Net2 design work is done. The LTC1545 extends the family by offering test mode capability. By replacing the 6-circuit LTC1544 with the 9-circuit LTC1545, the optional circuits TM (Test Mode), RL (Remote Loopback) and LL (Local Loopback) can now be implemented.

Figure 2 shows a typical application using the LTC1543, LTC1545 and LTC1344A. By just mapping the chip pins to the connector, the design of the interface port is complete. The chip set supports the V.28, V.35, V.36, RS449, EIA-530, EIA-530A or X.21 protocols in either DTE or DCE mode.

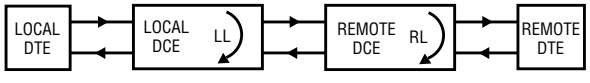

Figure 1. Serial network

Shown here is a DCE mode connection to a DB-25 connector. The mode-select pins, M0, M1 and M2, are used to select the interface protocol, as summarized in Table 1.

Table 1. Mode pin functions

LTC1543/LTC1545 Mode Name	M2	M1	M0
Not Used	0	0	0
EIA-530A	0	0	1
EIA-530	0	1	0
X.21	0	1	1
V.35	1	0	0
RS449/V.36	1	0	1
RS232/V.28	1	1	0
No Cable	1	1	1

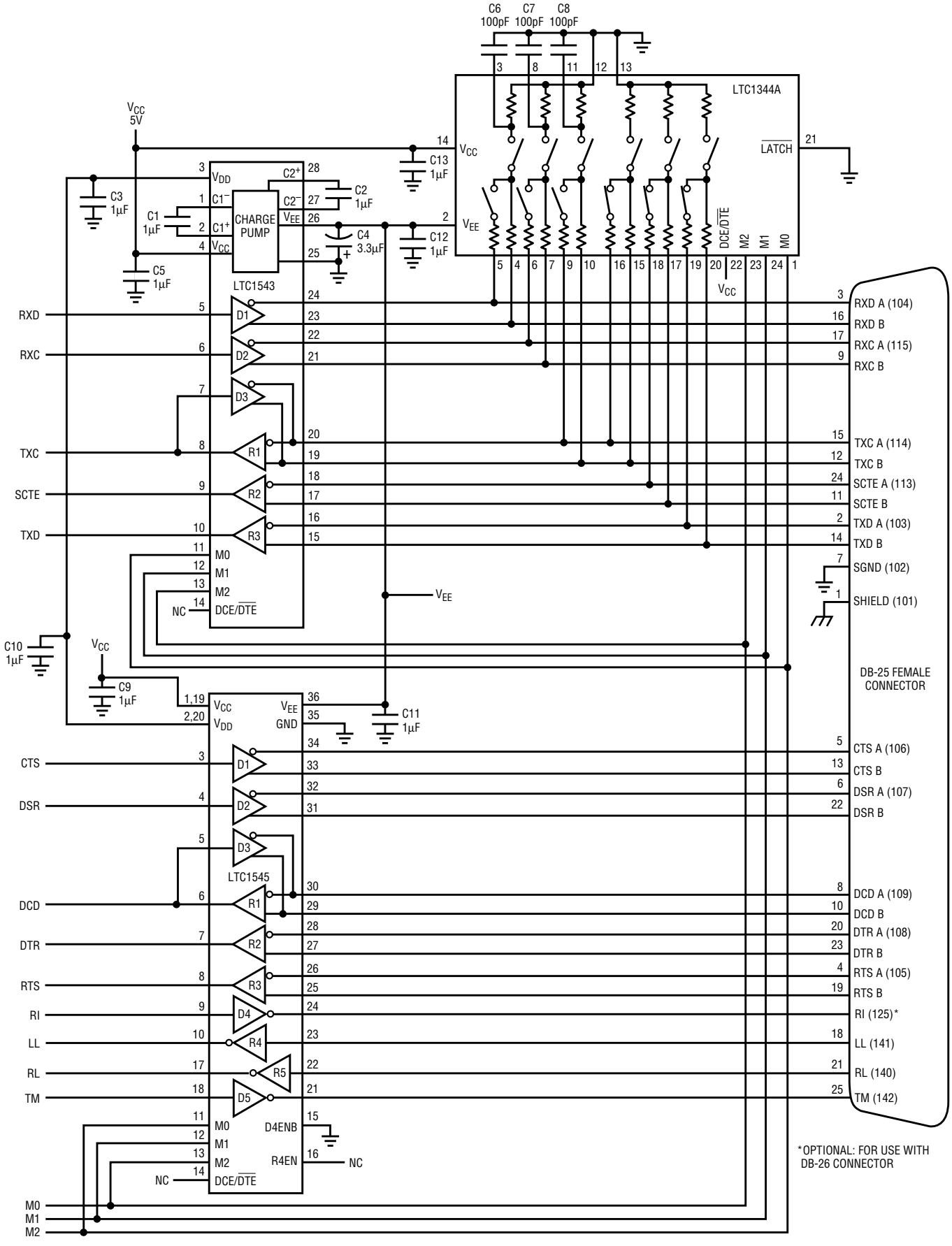

Figure 2. Typical application: Controller-selectable DCE port with DB-25 connector

Level Shift, continued from page 30

Fortunately, there is always synchronization information associated with video. A simple circuit can be used to DC restore voltage offsets produced by resistor mismatch, op amp offset or DC errors in the input video. Figure 2 shows the additional circuitry needed to perform this function. The LTC201A analog switch and C1 store the offset error during blanking. The clamp pulse should be 3µs or wider and should occur during blanking. It can conveniently be made by delaying the sync pulse with one shots. If the sync tip is clamped, the clamp pulse must start after and end before the sync pulse or offset errors will be introduced. The integrator made with the LT1632 adjusts the voltage at point B (see Figure 1) to correct the offset.

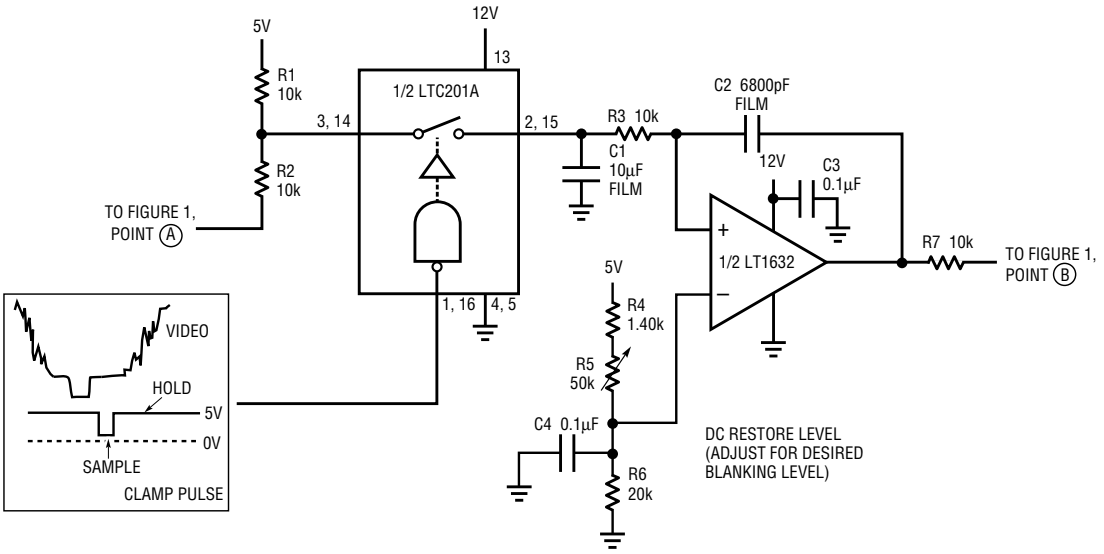

Figure 2. DC restore subcircuit

LTC2400, continued from page 4

configuration, the part performs one conversion, then automatically enters the power-down mode. The duration of the power-down mode is proportional to the capacitor value.

While $\overline{CS}$ is held high, the serial data out pin is high impedance. Once $\overline{CS}$ is pulled low, the part begins outputting data under the control of the SCLK pin.

This device can operate with either an internal or external serial clock. If the SCLK pin is left floating, the LTC2400 automatically detects this state and switches to internal clock mode. If the user drives the SCLK pin with his own clock, the part is automatically switched to external clock mode.

Many delta-sigma ADC's on the market include a PGA. These PGAs require that the designer deal with more device pins, status registers and timing sequences. Additionally, they limit the circuit's input range. For example, if the PGA's gain is 256 and the reference is 2.5V the resulting input range is 0mV to 10mV.

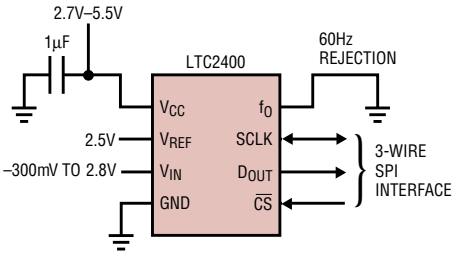

Figure 8. LTC2400 typical application

The LTC2400 provides better noise and TUE (total unadjusted error) performance than previous delta-sigma ADCs; moreover, the user is no longer confined to a 10mV input range. The input can still range between –12.5% × V_{REF} and 112.5% × V_{REF}. The eight MSBs determine the coarse input range. For example, if the eight MSBs = 00h, the input (V_{IN}) is in the range: 0 < V_{IN} < 10mV, whereas 01h corresponds to 10mV < V_{IN} < 20mV, and so on. This enables the LTC2400 to directly digitize a variety of low level sensors with large offsets.

The LTC2400 package is the smallest on the market (SO-8). This tiny chip combined with no external components enables the user to greatly reduce the board area required by existing designs.

Conclusion

The LTC2400 is the first of a family of delta-sigma converters from LTC. It offers a combination of the best characteristics of delta-sigma converters and conventional converters. Its attributes include latency-free operation and high precision INL, DNL and offset. It frees the user from adding external components and is easy to use. The on-chip sinc[4] filter reduces line frequency noise and its harmonics by 120dB, making it ideal for use in noisy environments. With only eight pins, an on-chip oscillator, 24-bit DNL, 4ppm INL and 10ppm TUE, the LTC2400 is the new state of the art in analog-to-digital conversion.

Notes:

1. Candy, J.C and G.C. Temes. "Oversampling Methods for A/D and D/A Conversion," in *Oversampling Delta-Sigma Data Converters*. IEEE Press, 1992.

2. Hauser, Max W. "Principles of Oversampling and A/D Conversion." *Journal of the Audio Engineering Society*, Vol. 39, No. 1/2 (January/February 1991) pp. 3–26.

New Device Cameos

LTC1436A/LTC1436A-PLL/ LTC1437A: High Efficiency, PLL-Lockable Switching Regulators

The LTC1436A/LTC1436A-PLL/ LTC1437A are high efficiency, low noise, synchronous switching regulators that drive external N-channel power MOSFETs in a phase-lockable, fixed frequency architecture and are ideal for notebook computers and battery-powered equipment requiring high frequency, low duty cycle operation.

The LTC1436A/LTC1436A-PLL/ LTC1437A have all of the outstanding features of the LTC1436/LTC1436-PLL/LTC1437 with a reduced minimum on-time of 300ns or less and improved noise immunity at low output voltages. With these improvements, high performance can be achieved at output voltages down to 1.3V with operating frequencies in excess of 250kHz and input supply voltages above 22V.

As with the originals, the improved parts feature the optional Adaptive Power™ output stage to provide good low current efficiency while maintaining constant frequency operation by selectively driving two topside N-channel MOSFETs sized for the appropriate load range. An auxiliary low dropout linear regulator is available to generate an additional supply that can be used as a CPU I/O supply or low noise audio supply. A secondary-winding-feedback/burst-disable input guarantees regulation regardless of the primary supply load by forcing continuous operation when needed.

Other features include a power-on reset timer that generates a logic-low output signal persisting for 65,536 clock cycles after the output is within 7.5% of the regulated output voltage, low dropout operation (99% duty cycle), a low-battery comparator with open-drain output and a wide supply range for operation from 3.5V to 36V.

The parts are available in 24-lead narrow SSOP for the LTC1436A and LTC1436A-PLL and 28-lead SSOP for the LTC1437A.

LTC1625 No R_{SENSE} Controller Now Available in Industrial Temperature Grade

An industrial temperature grade version of the LTC1625 No R_{SENSE}™ controller is now available for applications that require the enhanced temperature range (–40°C to 85°C). The LTC1625 provides true current mode control in step-down DC/DC converters without using a sense resistor. A current sense signal is obtained by monitoring the voltage drop across the MOSFET switches, making them perform double duty as current sense elements. Eliminating the sense resistor reduces board area, lowers costs and increases efficiency. Popular features from Linear Technology's other controllers have been incorporated, such as fixed frequency operation, N-channel MOSFET drive, Burst Mode™ operation, soft-start and output voltage programming. These features make the LTC1625 an excellent choice for DC/DC converter designs in a variety of applications that require the highest performance.

LTC1694: SMBus Accelerator

The LTC1694 is a dual active SMBus pull-up designed to enhance data-transmission speed and reliability under all specified SMBus loading conditions. It consists of two bilevel, hysteretic current source pull-ups that replace the pull-up resistors in a typical SMBus implementation. With the LTC1694, the user can connect multiple SMBus devices or use longer, more capacitive interconnects without compromising slew rates or penalizing bus performance.

Resistive pull-ups are used in many communications protocols that employ open-collector or open-drain drivers. Their simplicity is offset by the relatively slow rise times they afford when bus capacitance is high. Rise times can be improved by using lower pull-up resistance values, but the additional current through the low value resistors increases the low state bus voltage, decreasing noise margins. Slow rise times can seriously affect data reliability, enforcing a maximum practical bus speed well below the theoretical SMBus maximum transmission rate.

The LTC1694 overcomes these limitations by using bilevel, hysteretic current sources as pull-ups. During positive bus transitions, the current sources provide 2.2mA to quickly slew any parasitic bus capacitance. During negative transitions or steady DC levels, the current sources switch to 275µA to improve negative slew rate and improve low state noise margins. The fast rise times coupled with improved low state logic swings allow maximum transmission speed for any given bus loading conditions.

The LTC1694 is available in the 5-lead SOT-23 plastic surface mount package, requiring virtually the same board area as two surface mount resistors. The LTC1694 is specified for operation over the 0°C to 70°C temperature range.

LTC1530: High Power Synchronous Switching Regulator Controller with Current Limit in SO-8

The LTC1530 is a high power, high efficiency switching regulator controller optimized for 5V buck converter applications. A typical LTC1530 circuit can provide output currents of up to 20A. Packaged in an SO-8, the LTC1530 operates on a single supply of up to 14V. It includes a precision internal reference and an internal feedback system that can provide output voltage regulation of ±2% over temperature, load-current and line-voltage shifts.

The LTC1530 employs a synchronous switching architecture that drives two external N-channel output devices. It also senses current through the drain-source resistance (or on-

resistance) of the upper N-channel MOSFET, eliminating the need for an external, low value sense resistor. The current-limit trip point is set with a single external resistor; a temperature compensation circuit keeps the current-limit level constant as the external MOSFET $R_{DS(ON)}$ increases with temperature. The part also includes an on-chip soft-start capacitor; the soft-start slew rate is 0.4V/ms. It also has a thermal protection circuit that disables both internal gate drivers and reduces the supply current to 1mA when excessive die temperatures occur. In shutdown mode, the LTC1530 supply current drops to 45µA.

LTC1753: Programmable Synchronous Switching Regulator Controller

The LTC1753 is a high power, high efficiency, synchronous switching regulator controller that generates a digitally programmable output voltage between 1.3V and 3.5V. Step-down conversion is optimized for a 5V input. The internal 5-bit DAC accepts a parallel word and programs the output voltage from 1.3V to 2.05V in 50mV increments and from 2.1V to 3.5V in 100mV increments. The precision internal reference and feedback system provide an output voltage accuracy of ±1.5% at room temperature and ±2% (typical) over temperature, load current and line voltage shifts.

The LTC1753 uses a synchronous switching architecture with two external N-channel MOSFETs. It provides more than 14A of load current at efficiencies exceeding 90%. The LTC1753 senses output current through the on-resistance of the upper N-channel FET and provides adjustable current limit without the use of an external sense resistor. External MOSFET power dissipation is considerably reduced under output short-circuit conditions by an overcurrent protection scheme built into the LTC1753.

The free-running 300kHz oscillator frequency can be synchronized to a faster clock if desired. Soft-start eases inrush current and recovery from overload conditions. Protection features include overvoltage fault detection, overtemperature detection and a power-good signal when the output voltage is within ±5% regulation.

The LTC1753 is ideal for high power, tight tolerance microprocessors applications. It is available in 20-pin SO and SSOP packages.

The LTC1597/LTC1591: Ultra-accurate, Low Power 16- and 14-Bit Multiplying Current Output DACs Include On-Chip Resistors

Expanding LTC's family of current output, multiplying DACs are the pin-compatible 16-bit LTC1597 and 14-bit LTC1591. The LTC1597 features true 16-bit performance (DNL and INL, 1LSB maximum), low glitch impulse (2nV-s typical) and low supply power dissipation (10µW typical). The LTC1591 offers the same level of performance at 14-bit resolution. The LTC1597/LTC1591 can be configured for unipolar, 2-quadrant multiplying or for bipolar, 4-quadrant multiplying applications with no external resistors. For a fixed 10V reference input, the DAC unipolar output range is 0V to –10V and the DAC bipolar output range is ±10V. The LTC1597, coupled with LT1468 op amp, settles to within 0.0015% of full scale in 2µs. The LTC1597/LTC1591 have an asynchronous clear input that resets the output to zero scale. A second pair of parts, the LTC1597-1/LTC1591-1, resets to a midscale output. These devices also have a power-on reset. The LTC1597 and LTC1591 feature 16- and 14-bit parallel input data busses, respectively.

The LTC1597 and LTC1591 are designed for applications such as process control and industrial automation, direct digital waveform generation, software-controlled gain adjustment and automatic test equipment. Available in 28-pin SSOP or DIP packages, the LTC1597/LTC1591 operate on single 5V supplies.

LTC1258-2.5 Micropower Low Dropout Reference

The LTC1258-2.5 is a micropower bandgap reference that combines high accuracy and low drift with very low supply current and small package size. The combination of only 4µA quiescent current and low, 200mV Max dropout makes it ideal for battery-powered equipment.

This reference uses curvature compensation to obtain a low temperature coefficient and trimmed thin-film resistors to achieve high output accuracy. The reference can supply up to 10mA and sink up to 2mA, making it ideal for precision regulator applications. The LTC1258-2.5 is stable without an output bypass capacitor, but is also stable with capacitance up to 1µF. This feature is important in critical applications where PC board space is at a premium and fast settling is demanded.

This series reference provides supply current and power dissipation advantages over shunt references that must idle the entire load current to operate.

The LTC1258-2.5 is available in 8-pin SO and MSOP packages.

for the latest information on LTC products, visit www.linear-tech.com

For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

DESIGN TOOLS

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FilterCAD™ 2.0 CD-ROM — This CD is a powerful filter design tool that supports all of Linear Technology's high performance switched capacitor filters. Included is FilterView™, a document navigator that allows you to quickly find Linear Technology monolithic filter data sheets, the FilterCAD manual, application notes, design notes and *Linear Technology* magazine articles. It *does not* have to be installed to run FilterCAD. It is not necessary to use FilterView to view the documents, as they are standard .PDF files, readable with any version of Adobe Acrobat™. FilterCAD runs on Windows® 3.1 or Windows 95. FilterView requires Windows 95. The FilterCAD program itself is also available on the web and will be included on the new LinearView™ CD. Available at no charge.

Noise Disk — This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp. Available at no charge

SPICE Macromodel Disk — This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models and a demonstration copy of PSPICE™ by MicroSim. Available at no charge

SwitcherCAD™ — The SwitcherCAD program is a powerful PC software tool that aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. 144 page manual included. $20.00

SwitcherCAD supports the following parts: LT1070 series: LT1070, LT1071, LT1072, LT1074 and LT1076. LT1082. LT1170 series: LT1170, LT1171, LT1172 and LT1176. It also supports: LT1268, LT1269 and LT1507. LT1270 series: LT1270 and LT1271. LT1371 series: LT1371, LT1372, LT1373, LT1375, LT1376 and LT1377.

Micropower SwitcherCAD™ — The MicropowerSCAD program is a powerful tool for designing DC/DC converters based on Linear Technology's micropower switching regulator ICs. Given basic design parameters, MicropowerSCAD selects a circuit topology and offers you a selection of appropriate Linear Technology switching regulator ICs. MicropowerSCAD also performs circuit simulations to select the other components which surround the DC/DC converter. In the case of a battery supply, MicropowerSCAD can perform a battery life simulation. 44 page manual included. $20.00

MicropowerSCAD supports the following LTC micropower DC/DC converters: LT1073, LT1107, LT1108, LT1109, LT1109A, LT1110, LT1111, LT1173, LTC1174, LT1300, LT1301 and LT1303.

Technical Books

1990 Linear Databook, Vol I —This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

1992 Linear Databook, Vol II — This 1248 page supplement to the 1990 Linear Databook is a collection of all products introduced in 1991 and 1992. The catalog contains full data sheets for over 140 devices. The 1992 Linear Databook, Vol II is a companion to the 1990 Linear Databook, which should not be discarded. $10.00

1994 Linear Databook, Vol III —This 1826 page supplement to the 1990 and 1992 Linear Databooks is a collection of all products introduced since 1992. A total of 152 product data sheets are included with updated selection guides. The 1994 Linear Databook Vol III is a companion to the 1990 and 1992 Linear Databooks, which should not be discarded. $10.00

1995 Linear Databook, Vol IV —This 1152 page supplement to the 1990, 1992 and 1994 Linear Databooks is a collection of all products introduced since 1994. A total of 80 product data sheets are included with updated selection guides. The 1995 Linear Databook Vol IV is a companion to the 1990, 1992 and 1994 Linear Databooks, which should not be discarded. $10.00

1996 Linear Databook, Vol V —This 1152 page supplement to the 1990, 1992, 1994 and 1995 Linear Databooks is a collection of all products introduced since 1995. A total of 65 product data sheets are included with updated selection guides. The 1996 Linear Databook Vol V is a companion to the 1990, 1992, 1994 and 1995 Linear Databooks, which should not be discarded. $10.00

1997 Linear Databook, Vol VI —This 1360 page supplement to the 1990, 1992, 1994, 1995 and 1996 Linear Databooks is a collection of all products introduced since 1996. A total of 79 product data sheets are included with updated selection guides. The 1997 Linear Databook Vol VI is a companion to the 1990, 1992, 1994, 1995 and 1996 Linear Databooks, which should not be discarded. $10.00

1990 Linear Applications Handbook, Volume I — 928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels. $20.00

1993 Linear Applications Handbook, Volume II — Continues the stream of "real world" linear circuitry initiated by the 1990 Handbook. Similar in scope to the 1990 edition, the new book covers Application Notes 40 through 54 and Design Notes 33 through 69. References and articles from non-LTC publications that we have found useful are also included. $20.00

1997 Linear Applications Handbook, Volume III — This 976 page handbook maintains the practical outlook and tutorial nature of previous efforts, while broadening topic selection. This new book includes Application Notes 55 through 69 and Design Notes 70 through 144. Subjects include switching regulators, measurement and control circuits, filters, video designs, interface, data converters, power products, battery chargers and CCFL inverters. An extensive subject index references circuits in LTC data sheets, design notes, application notes and *Linear Technology* magazines. $20.00

1998 Data Converter Handbook — This impressive 1360 page handbook includes all of the data sheets, application notes and design notes for Linear Technology's family of high performance data converter products. Products include A/D converters (ADCs), D/A converters (DACs) and multiplexers—including the fastest monolithic 16-bit ADC, the 3Msps, 12-bit ADC with the best dynamic performance and the first dual 12-bit DAC in an SO-8 package. Also included are selection guides for references, op amps and filters and a glossary of data converter terms. $10.00

Interface Product Handbook — This 424 page handbook features LTC's complete line of line driver and receiver products for RS232, RS485, RS423, RS422, V.35 and AppleTalk® applications. Linear's particular expertise in this area involves low power consumption, high numbers of drivers and receivers in one package, mixed RS232 and RS485 devices, 10kV ESD protection of RS232 devices and surface mount packages. Available at no charge

Power Solutions Brochure — This collection of circuits contains real-life solutions for common power supply design problems. There are over 88 circuits, including descriptions, graphs and performance specifications. Topics covered include battery chargers, PCMCIA power management, microprocessor power supplies, portable equipment power supplies, micropower DC/DC, step-up and step-down switching regulators, off-line switching regulators, linear regulators and switched capacitor conversion. Available at no charge

Data Conversion Solutions Brochure — This 64 page collection of data conversion circuits, products and selection guides serves as excellent reference for the data acquisition system designer. Over 60 products are showcased, solving problems in low power, small size and high performance data conversion applications—with performance graphs and specifications. Topics covered include ADCs, DACs, voltage references and analog multiplexers. A complete glossary defines data conversion specifications; a list of selected application and design notes is also included. Available at no charge

Telecommunications Solutions Brochure — This collection of circuits, new products and selection guides covers a wide variety of products targeted for the telecommunications industry. Circuits solving real life problems are shown for central office switching, cellular phone, base station and other telecom applications. New products introduced include high speed amplifiers, A/D converters, power products, interface transceivers and filters. Reference material includes a telecommunications glossary, serial interface standards, protocol information and a complete list of key application notes and design notes. Available at no charge

continued on page 40

DESIGN TOOLS, continued from page 39

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